ETL Flipped Module Proposal

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Contents

1 Introduction to the Flipped Module Design

This document describes an alternative of the ETL module and service hybrid design to the TDR design. We undertook the detailed design of the readout board, moving from the initial design in the TDR to layout of boards for a first prototype. The primary challenge in the design is the limited space, with the TDR design assuming a z-thickness of less than 7 mm for the combined thickness for a power board stacked on the readout board. Developing a detailed design within this constraint introduces significant design complications. Studying that challenge led us to propose a modification to the positioning of the boards and a modification to the module, which we call the Flipped Module design. This provides significantly more space for both the readout board and the power board, and it is described below.

In this proposal the LGAD silicon sensor is located below the read out chip (ETROC), essentially flipping the TDR module on its head. A PCB can be mounted (glued) on top of the ETROC, allowing for a board-to-board connection to the readout board (RB). Signals, LV and bias voltage (BV) are distributed from the RB to the module via these board-to-board and spring connectors. The ETROC and the LGAD sensor are connected to the PCB through wire bonds.

We foresee three different versions of the RB: covering 3 (6), 6 (12) and 7 (14) full (half) modules. Each full module consists of two LGAD sensors and four readout chips (ETROC).

The expected radiation environment for various regions are shown in Table 1. To deal with higher occupancy in high-$|\eta|$ regions the innermost part of the ETL disk ($r < 425$ mm $\equiv |\eta| > 2.65$) will be populated by 3-module readout boards. The rest of the disk is organized such that the area coverage of the detector with sensors is optimized. The layout of modules and service hybrids on the surface of the ETL wedges is presented in Figure 3. Very good coverage between $1.7 < |\eta| < 2.8$ is achieved, without the need for half-sized modules. We reserve an area of the width of RB and PB with a depth of 50 mm at the outer edge of the disks for MT connectors as well as LV and BV distribution, shown in Fig. 2. The main difference w.r.t. the TDR design in terms of service hybrids is the placement of the RB on top of the modules, instead of the power board. The RBs are powered either from above or below (powered from above shown in Fig. 3).

Table 1: Nominal radiation doses and fluences at various locations of the timing layers after 3000 fb^{-1}. The fluence is normalized to 1 MeV neutron equivalent in silicon. Numbers from CERN-LHCC-2019-003.

Region	η	R (cm)	z (cm)	Fluence (cm^{-2})	Dose (kGy)
barrel	0.0	116	0	1.65×10^{14}	18
barrel	1.15	116	170	1.80×10^{14}	25
barrel	1.45	116	240	1.90×10^{14}	32
endcap	1.6	127	303	1.5×10^{14}	19
endcap	2.0	84	303	3.0×10^{14}	50
endcap	2.5	50	303	7.5×10^{14}	170
endcap	3.0	31.5	303	1.6×10^{15}	450

2 Changes to the Module Design

In this proposal, no half size modules are foreseen. The modules themselves have a changed structure, shown in Figure 1:

- A thicker carrier (approx. 1 mm) made out of Aluminium nitride (AlN) or Aluminium oxide (alumina)
- The LGAD sensor is directly mounted to the carrier, below the ETROC
- The LGAD (BV) and ETROC (signals and LV) are wire bonded to a PCB that covers the module
- The module is connected to the readout board via board-to-board connectors

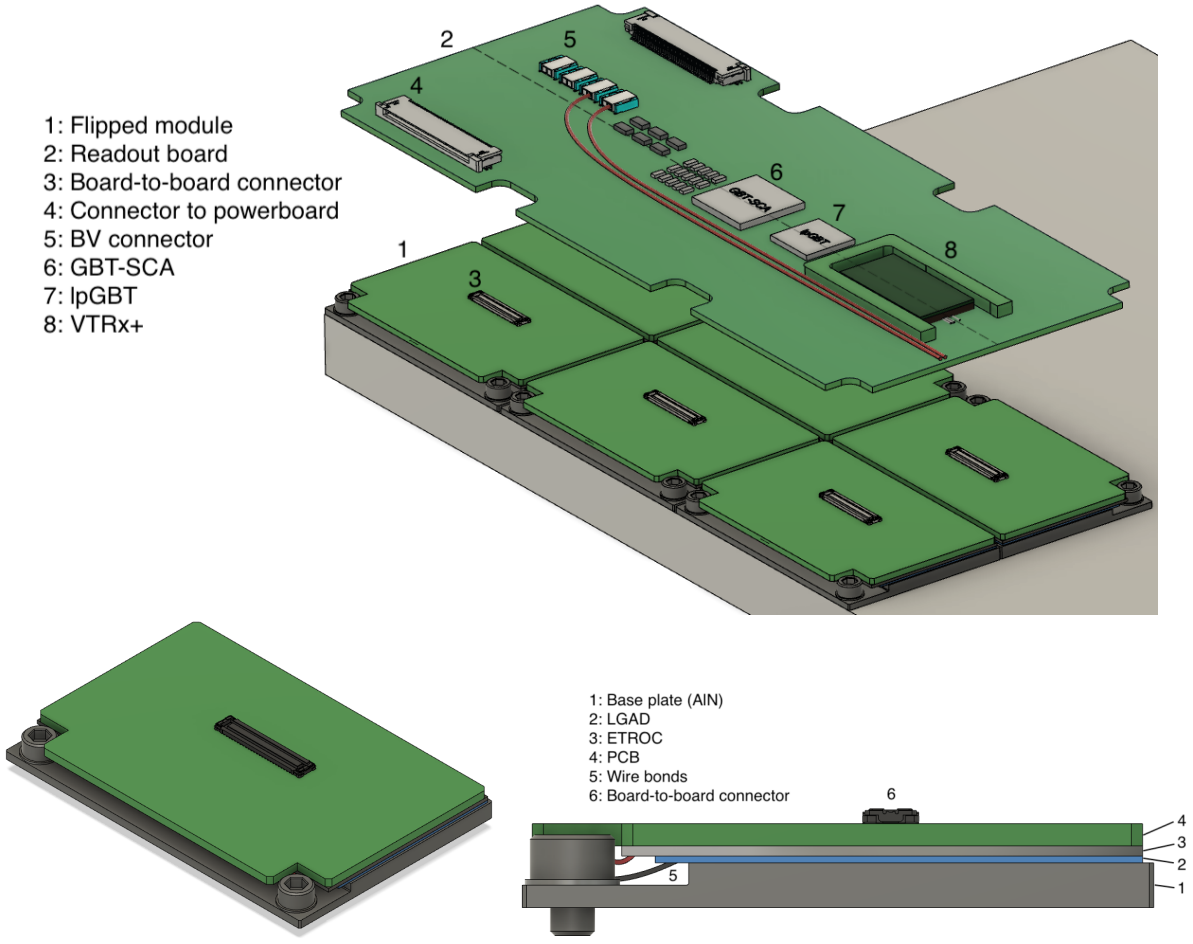

Figure 1: Top: Partially exploded views of the module-RB sandwich showing its various components. Bottom: View of a half module in the flipped configuration, with the LGAD sensor below the ETROC.

Table 2: List of the number of each type of component used in the full ETL detector.

Component type	Number per wedge (avg)	Total number
LGADs	930	14,880
ETROCs	1,860	29,760
2-sensor (full size) modules	465	7,440
1-sensor (half size) modules	0	0
total service hybrids	86.5	1,384
3-module service hybrids	28.5	456
6-module service hybrids	26.5	424
7-module service hybrids	31.5	504
lpGBTs, VTRX, SCA	86.5	1,384
DC-DC converters	915	14,640

Table 3: Stack-up height of the module-readout board sandwich. The space taken up by the VTRx+ is the minimum z space on top of the RB PCB that will be available for BV connectors and routing of services.

Component	Approx. thickness
AlN base plate	1–2mm
LGAD sensor	0.3mm
ETROC	0.5mm
Module PCB	0.5mm
Board-to-board connector	0.7mm
Readout board PCB	1mm
VTRx+	2.5mm
Total	6.5–7.5mm

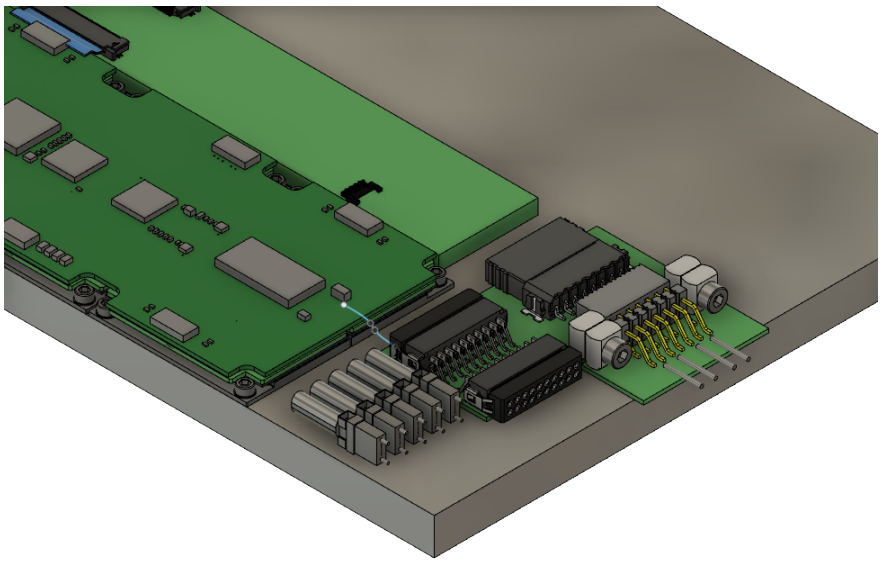

Figure 2: Mini-patch-panel at the end of each row of RBs and PBs.

3 Service Hybrid Requirements

The proposal does not directly impact the design of the power board. The service hybrid corridor assumed to be available for the PB is 29.5mm wide, and the full height of approximately 7.0 − −8.5 mm is available for the PB, an increase in the vertical space available for the PB which may have benefits for efficiency or other aspects of the power board design. In this proposal, the only services routed on top of the PB are the LV and DSS cables. The connection from PB to RB is yet to be defined, but some options under consideration are:

- Connection with rigid connectors, e.g. 100-mil single row right angle headers
- Connection with short patch cables, e.g. DF57
- Connection with a short flex-rigid board, with board-to-board connectors on both the power-board and readout board.

4 Geometric Coverage

We optimize the placement of modules and readout boards to achieve highest possible coverage of the ETL disk, without the need for half size modules. The ETL disk is assumed to be limited by $r_{\text{inner}} = 315$ mm and $r_{\text{outer}} = 1185$ mm, depicted by the red circles in Figure 5, corresponding to $1.659 \leq |\eta| \leq 2.950$ for an ETL position of $z = 3$ m. Modules on the front and back face of each disk are arranged such that the area not covered by a sensor is minimized. The two different arrangements are shown on the left and right of Figure 5.

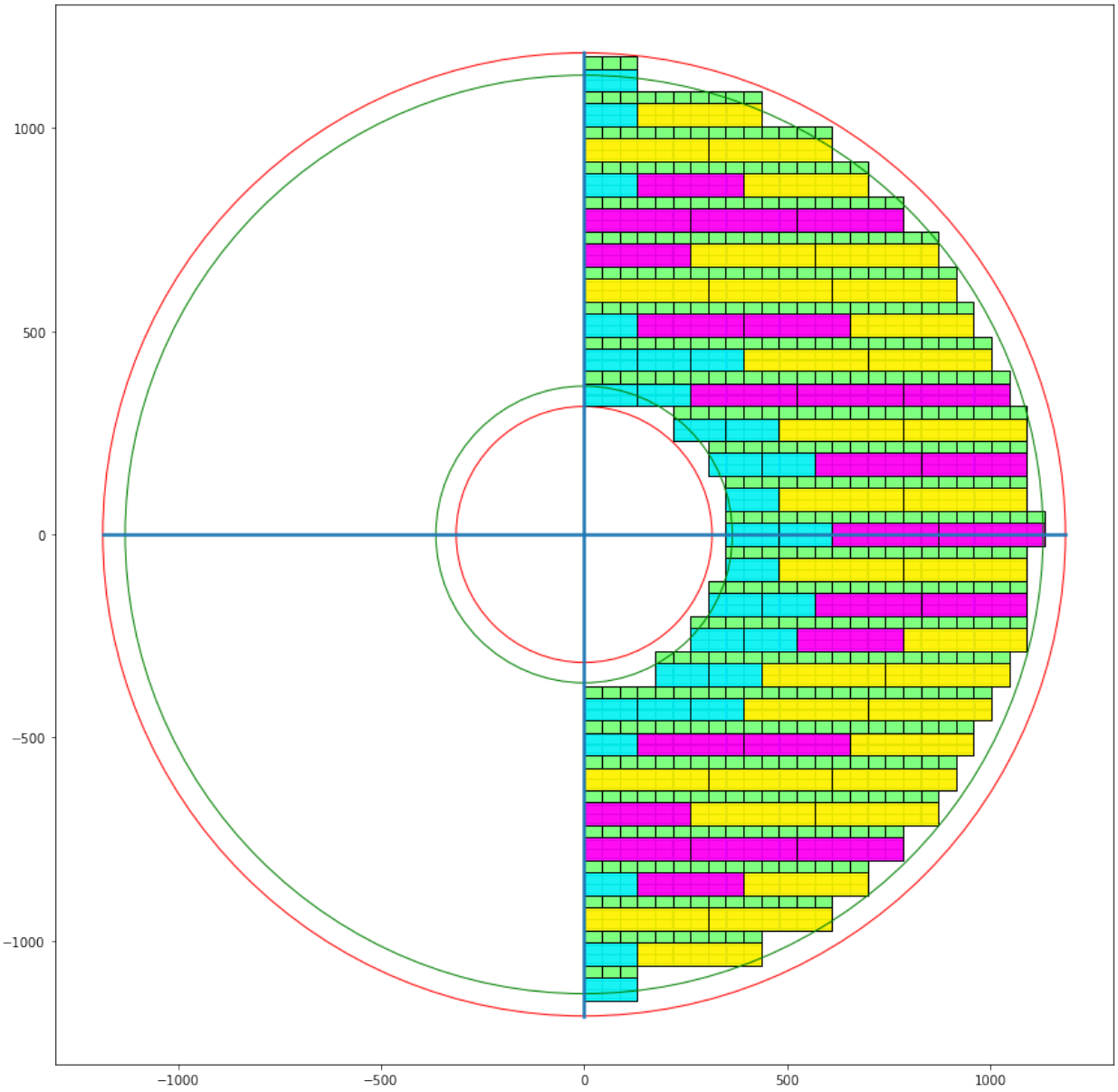

Figure 3: Layout of various kinds of RBs on an ETL half-disk. The red and green circles reflect the mechanical envelope of the ETL disk and the area between $1.7 < |\eta| < 2.8$, respectively. Cyan, pink and yellow rectangles correspond to 3-, 6-, and 7-module readout boards. The green rectangles indicate the reserved space above the RB for the power boards and LV services.

In order to measure the coverage of the proposed module layout we use LGAD sensor dimensions of 22.0×42.5 mm, and a full module of size 56.5×43.1 mm. A 0.5 mm gap between each module is assumed, and the channel for the power board is taken to be 29.5 mm wide. Each side of the ETL detector is made of two disks (four faces) that are shifted by 2 mm in x and y in order to also cover the inter-sensor gaps.

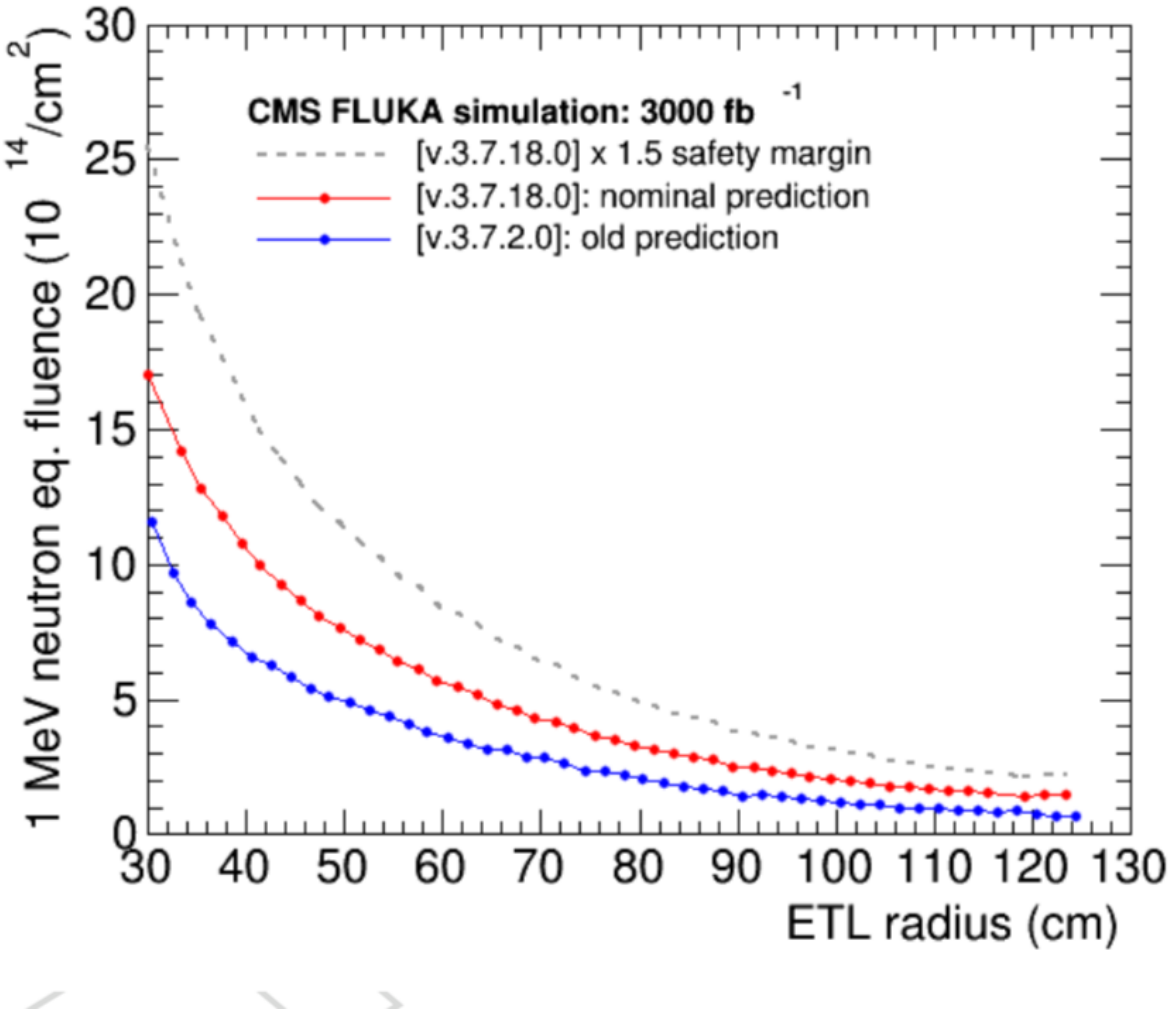

Figure 4: Fluence prediction in ETL for an integrated luminosity of 3000 fb^{-1} from the FLUKA simulations.

Table 4 shows the acceptance and geometric coverage of four different configurations of ETL modules on the disk. The acceptance is measured by propagating muons produced at the center of CMS with $p_T > 5$ GeV and a flat η distribution through the CMS magnetic field to the ETL detector. The different configurations correspond to the amount of space that is not covered by sensors at the outer edge of the disk in order to accommodate connectors (and potentially a mini-patch-panel for BV, LV and DSS). The "optimal" configuration corresponds to the case where modules are placed up to the most outer edge of the disk, leaving no additional space for connectors. In this case, 91% of the area of the disk is covered by at least one sensor. If 50, 65 or 85mm of space, measured along the x-axis from the modules, is kept free of modules, this geometric coverage reduces to 84–81%. However, due to the flat η distribution that is used for the acceptance measurement with muons, the acceptance only reduces to 87–86%. For the region $1.70 < |\eta| < 2.80$ more than 97% of muons intersect at least one sensor in any of the configurations. An example of tracks and

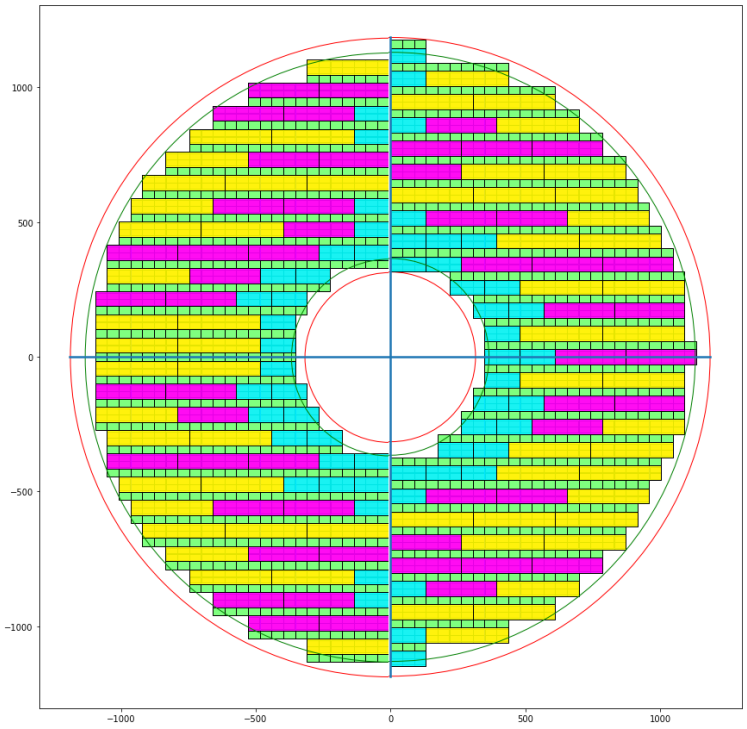

Figure 5: Two half disks of the ETL detectors. The red and green circles reflect the mechanical envelope of the ETL disk and the area between $1.7 < |\eta| < 2.8$, respectively. Cyan, pink and yellow rectangles correspond to 3-, 6- and 7-module readout boards. The green rectangles indicate the reserved space for the power boards and LV services.

intersections with ETL sensors is shown in Fig. 6. The majority of muons not producing any hit pass through uncovered areas at the edge of the ETL disks. If the rapidity window is narrowed to $2.0 < \eta < 2.5$, more than 99% of the muons intersect at least one of the sensors.

5 Services

At most five service hybrids are arranged in one row on the ETL disk, shown in Fig. 5. Such a configuration is shown in Fig. 7. LV cables can be routed on top of the PB, while the optical fibre bundles and BV cables will be routed on top of the RB. MT connectors for the fibres are located at

Table 4: Acceptance for muons and geometric coverage of different configurations.

Configuration	$1.66 < \|\eta(\mu)\| < 2.95$		$1.70 < \|\eta(\mu)\| < 2.80$		Geometric coverage	
	≥ 1 hit	≥ 2 hits	≥ 1 hit	≥ 2 hits	total	w.r.t. optimal
optimal	0.91	0.79	> 0.99	0.91	0.91	1.00
50mm	0.87	0.75	0.99	0.91	0.84	0.924
65mm	n/a	n/a	n/a	n/a	0.83	0.915
85mm	0.86	0.75	0.97	0.90	0.81	0.894

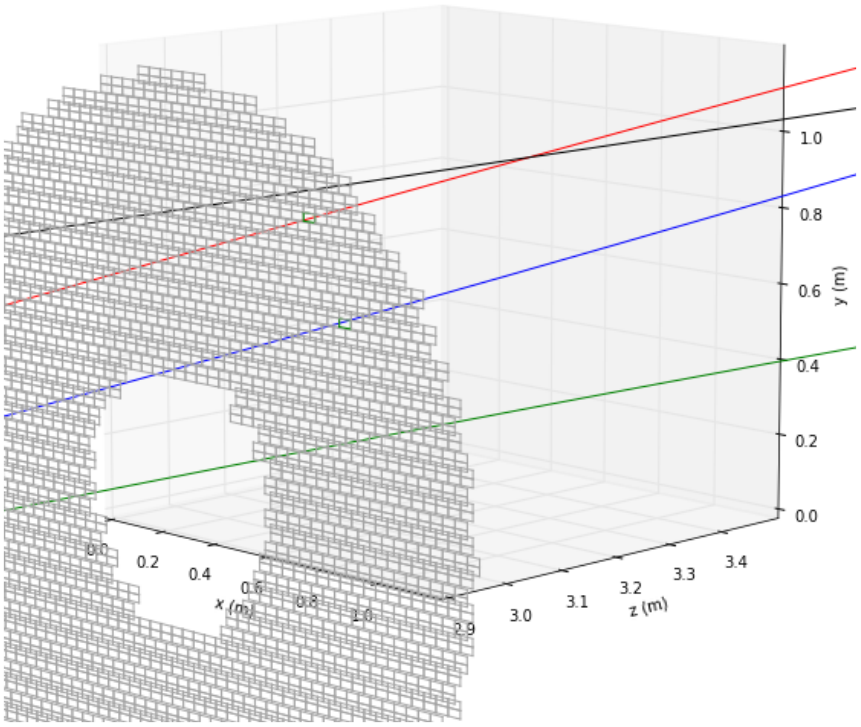

Figure 6: Tracks of three muons (red, blue, green) originating from the CMS interaction point, propagated through the CMS magnetic field. Sensors of the first two faces of the ETL detector are shown. Sensors that intersect the muon tracks are marked in green. The green track passes the ETL detector without an intersection at the outer (low-η) edge of disk.

the end of each row, and can be accompanied by small patch panels for LV, BV and DSS connection.

Moving the LV and BV connectors from the patch panel PP0 to the proposed mini patch panels at the periphery on the disk has the advantage that the connectors are easily accessible. In the TDR concept the PP0 is located behind the two discs below the cooling lines, shown in Fig. 8. This makes connecting the cables to PP0 very difficult because it would be in the shadow of already installed discs. Additionally, if no space for PP0 behind the disks is needed, the available space in z-direction for the modules/service hybrids increases from 7 mm to about 8.5 mm. A concept of the alternative mini patch panels at the end of each row of modules and service hybrids is shown in Fig. 2.

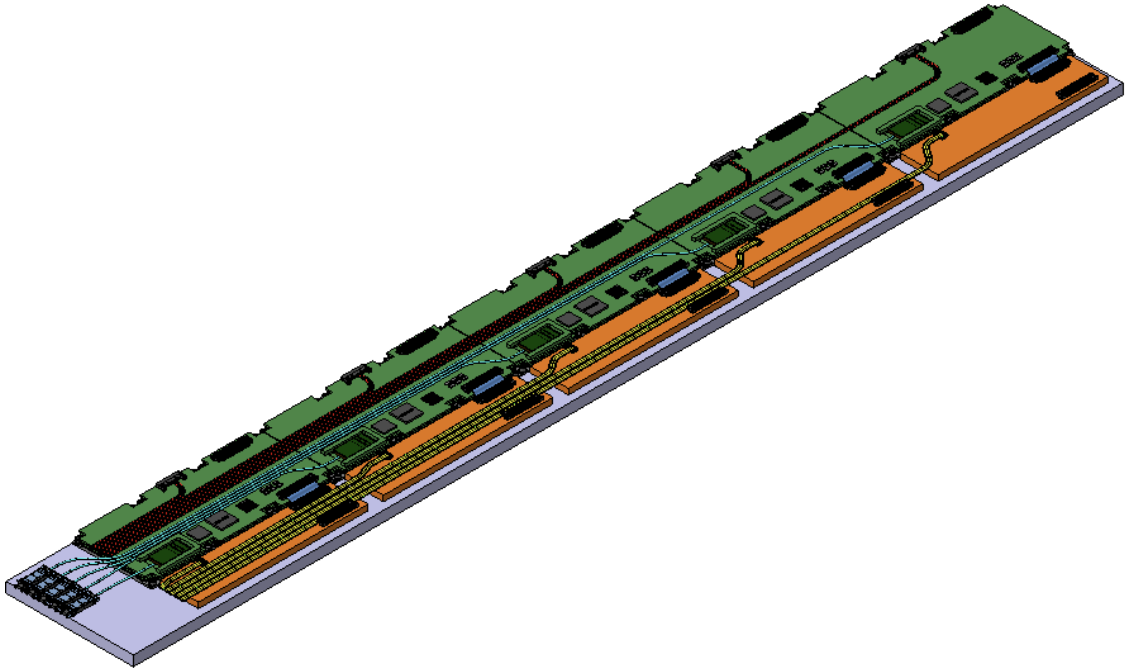

Figure 7: Representation of the longest row of service hybrids, accommodating all necessary services (BV, LV, fibre bundles).

6 Assembly and testing

With the proposal at hand it is possible to assemble "super-modules" of the size of one readout board, which can then be tested and only subsequently get mounted on the ETL disk. The assembly process would therefore be greatly simplified once the modules are assembled.

A possibility exists also for a futher level of "super-module" assembly, in that the readout board and power board and modules could all be connected together as a standalone apparatus, which can be independently tested in the assembly site prior to installation on the Dee.

There are different possible mechanical arrangements to build this super assembly, which are described in the following sections.

In either design, individual modules connected one-by-one to the readout board. Each of these modules is attached through board-to-board connectors to the readout board with no other rigid attachment points, so any ill effects from thermal expansion and misalignment are expected to be very small.

6.1 AlN Attached to Cooling Plate

In the baseline design, similar to the TDR or as shown in other diagrams of this document, the modules themselves are screwed to the aluminum plate, and the readout board is attached to them separately. In this design, the force to keep the modules in contact with the cooling plate

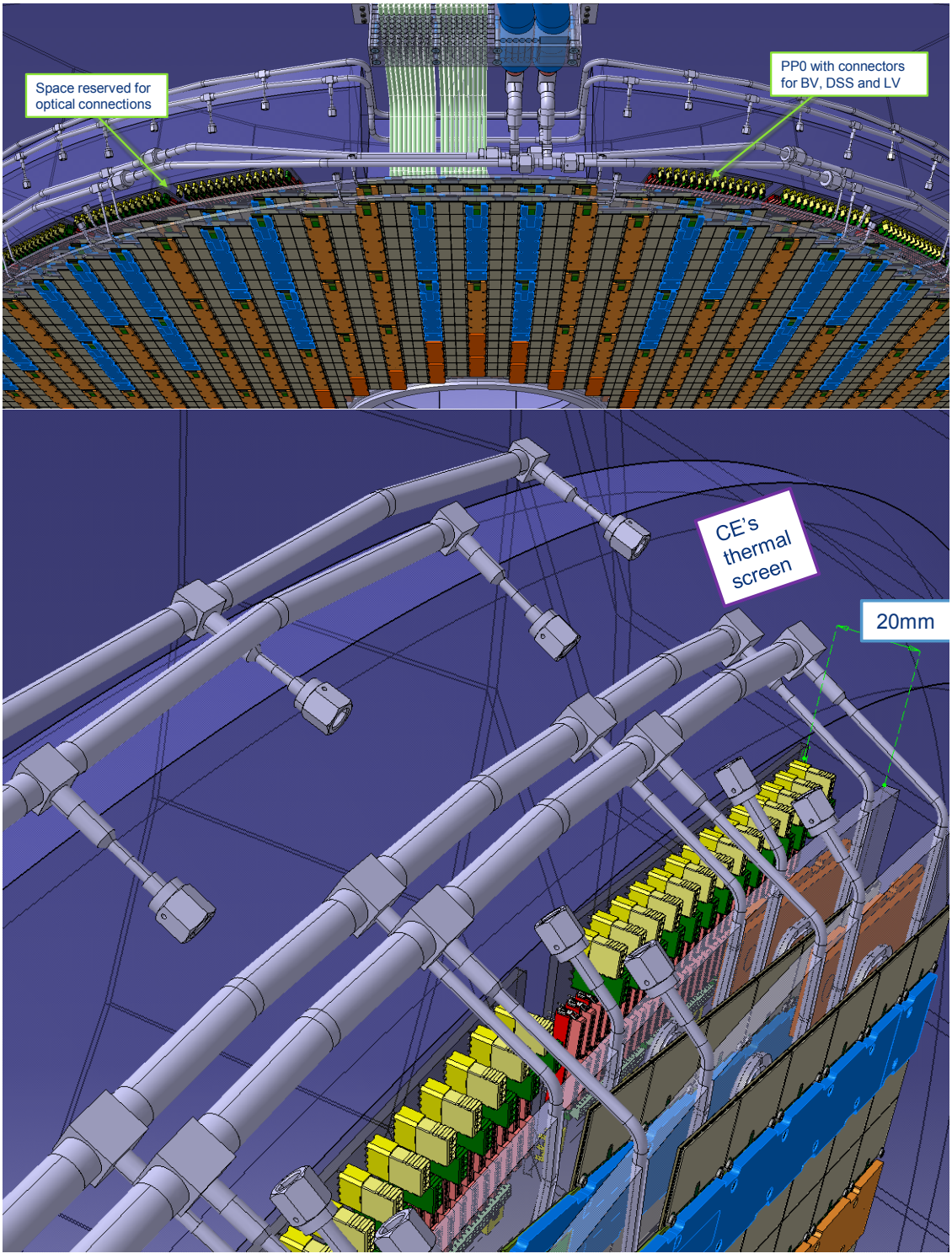

Figure 8: Conceptual layout and location of the TDR PP0 behind the two disks.

comes from the screw connection at the periphery of the module.

Some possible concerns about this design in the flipped module proposal are:

- The thickness of the AlN plate required to ensure mechanical integrity and good contact between the module and the cooling plate

- Maintaining alignment and minimizing strain between the collection of board-to-board connectors under thermal expansion. Since the modules are attached to the aluminum cooling plate, they will move with its coefficient of thermal expansion, while having to maintain good electrical and mechanical contact through the board-to-board connectors of the readout-board, which will have very different thermal properties.

6.2 Readout Board Attached to Cooling Plate

An alternative idea, following a suggestion from Sergei Lusin, uses the readout board as the attachment point to the cooling plate, with the readout board PCB itself providing the downward force necessary to keep the modules themselves in contact with the cooling plate rather than the screws directly.

A flat spacer (e.g. of plastic, kapton, fr4) with cutouts for the board-to-board connectors is placed in between the modules and the bottom surface of the readout board. The thickness of the spacer would be very slightly larger than the board-to-board connector stack height, which allows it to transfer force on the readout board more evenly across the surface area of the module, rather than being concentrated on the connectors themselves.

Screws would then be installed to connect the readout-board itself to the aluminum disk, rather than the modules. The modules would then only be rigidly connected to the FR4 readout-board, which has very similar coefficients of thermal expansion to the modules themselves. The readout board could have e.g. slotted screw holes which can absorb some misalignment due to thermal expansion.

A simplified diagram of such a design is shown in Figure 9.

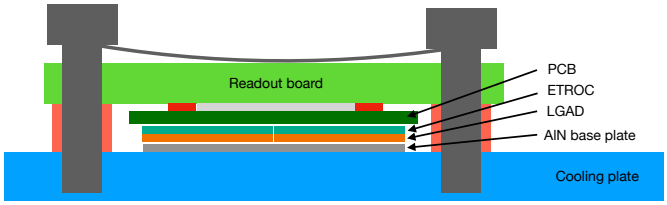

Figure 9: A possible scheme for attaching the readout board and modules to the cooling plate, by screwing the readout board itself into the aluminum cooling plate. Some additional metal pieces can be used to strengthen the readout board and better distribute force across the surface. Standoffs are installed between the readout-board and the cooling plate to prevent over-tightening.

In this design, since the modules themselves are not directly bonded to the aluminum disk, differences in coefficients of thermal expansion are not directly contributing to strain on the board-to-board connectors and concerns of strain are significantly lessened.

7 Potential challenges

The following potential challenges have been identified:

- The space on top of the ETL modules was reserved for service routing, which is now occupied by the readout board. Nevertheless, we have mapped out a detailed plan for the routing that fits.

- Thermal expansion problems of the module components: this will be tested in depth, but $\Delta T > 200C$ during bump bonding of silicon to PCBs has not caused any problems so far. This is not a full test of issues for a glued (rather than bump bonded) connection, however, and that test should be done by experts e.g. at UNL or UCSB. A back of the envelope calculation of the difference in thermal expansion between the FR4 and Silicon shows roughly 10μm difference in expansion across a 100K temperature difference, which is expected to be acceptable, but further tests are required to prove this.

- Thermal conductivity: Calculations show that the temperature gradient within the silicon sensor is below 0.1K, and the temperature difference between LGAD and ETROC (across bumps) is below 1K. See Appendix A for details on this calculation.

- Thermal runaway of sensors: Should be less of a problem in this design as the sensor is directly connected to cooling.

- Alignment and insertion force of board-to-board connectors: We ordered connectors and will conduct studies soon.

8 Summary

The presented change of the ETL module and service hybrid design has several advantages over the TDR design:

- Less space restrictions for RB and PB, especially vertically, giving more freedom in choice of components such as capacitors and inductors, and also allowing the power board to increase in thickness and possibly realize improvements in the embedded inductors

- Direct connection of RB to the module without flexi circuits, facilitating the assembly and testing processes

- PCB on modules allows for placement of components (e.g. bypass capacitors) close to the sensor and ETROCs

- No need for half sized modules
- Required stacking height of down to 7 mm seems feasible

Appendices

A Temperature Gradient Calculation

One concern of the flipped module design was the possible introduction of a temperature gradient inside of the sensor, due to the changes in heat flow. In the normal design, the ETROC heat is dissipated directly through the AlN plate, while in the flipped-module design the ETROC heat must dissipate through the bump-bonds, into the sensor, and then into the AlN plate.

This introduces the possibility of temperature non-uniformity inside of the LGAD sensor. To investigate this concern, some simplified calculations were done independently by David Stuart and Frank Golf. Different assumptions about material thicknesses and conductivity were made in each calculation, but the methods are the same and the calculation was cross-checked by a third program.

The main conclusion of these calculations is that the principal concern of temperature gradients existing in the silicon, is negligible. A temperature difference of only 0.02K is predicted between the hottest and coldest parts of the sensor. This is due in large part to the relatively high thermal conductivity of silicon.

In both calculations, the common set of assumptions was:

- AlN Thickness = 2mm
- Size of a sensor pad = 1.3mm
- Number of bumps bonds per ETROC = 256
- ETROC Power = 1 Watt
- Bump diameter = 90 μm
- Area of an LGAD = $(1.3\text{mm})^2 \times 256$ bumps $\times 2$ ETROCs$= 865.28$ mm^2

The differences in assumptions between the two calculations are:

Parameter	**Golf**	**Stuart**	**Unit**
Solder bump conductivity	70	60	W/m·K
Solder bump height	100	150	μm
Silicon sensor conductivity	150	191	W/m·K
Silicon sensor thickness	300	200	μm
Epoxy conductivity	0.22	1.33	W/m·K
Epoxy thickness	500	1000	μm
AlN conductivity	160	200	W/m·K

The results of the two calculations are:

Parameter	Golf	Stuart	Unit
Single Bump Conductance	0.004	0.003	W/K
Single Bump Δt	0.8772	1.5351	K
All bumps Conductance	1.140	0.651	W/K
All bumps Δt	0.8772	1.5351	K
Sensor Conductance	432.640	826.342	W/K
Sensor Δt	0.0046	0.0024	K
Epoxy Conductance	0.381	1.151	W/K
Epoxy Δt	5.2532	1.7379	K
AlN Conductance	69.222	86.528	W/K
AlN Δt	0.0289	0.0231	K
Silicon (horizontal) Conductance	0.045	0.038	W/K
Silicon (horizontal) Δt	0.0217	0.0256	K

David's original notes go into detail on the methods and assumptions used in producing the calculation, and can be found at `http://stuart.physics.ucsb.edu/Lgbk/pub/E40756.dir/E40756.html`. His calculations are saved in a root macro which can be found at Calc.C. Backup copies of both the notes and root script are copied into the Git repository of this document at `https://github.com/bu-etl/readout-board-docs`

Frank's calculation can be found in a python script, accessible at: `https://github.com/bu-etl/readout-board-docs/blob/master/scripts/thermal_module.py`

A unified calculation used to cross-check the two can be found in a Julia script at: `https://github.com/bu-etl/readout-board-docs/blob/master/scripts/thermal_module.jl`