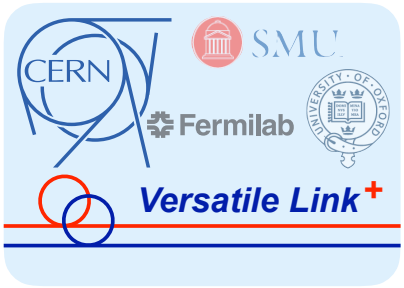

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Application Note

VTRx+ Receiver Saturation and Mitigation

Abstract

The GBTIA trans-impedance amplifier used in the VTRx+ receiver is designed to be sensitive to small photocurrents generated by degraded photodiodes in harsh radiation environments. The drawback is that, due to its limited dynamic range, GBTIA can saturate with large input optical modulation amplitudes. This receiver saturation may effect the uplink performance before any errors are measured in the downlink, because in typical Tx/Rx configuration lpGBT recovers the clock from the downlink datastream. This application note explains the conditions required for the saturation to occur and provides simple mitigation guidelines.

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Document History

Rev. No	*Date*	*Pages*	*Description of Changes*
1.1	3 July 2024	*4*	Updated figure captions to clarify what signal is being shown in the figures 2 and 3

Saturation of the VTRx+ receiver

VTRx+ receiver consists of InGaAs photodiode and GBTIA trans-impedance amplifier. GBTIA is sensitive to photo currents in the 10 µA range, which is important feature as photodiodes lose their responsivity under particle irradiation. InGaAs photodiodes are also prone to high leakage currents when exposed to high levels of displacement damage. GBTIA is designed to handle leakage currents up to 1 mA. However, as the dynamic range of the amplifier circuitry is limited, it is possible that high optical input power, i.e. high modulated power, can saturate the receiver. This is illustrated in the example bathtub curve shown in Fig. 1.

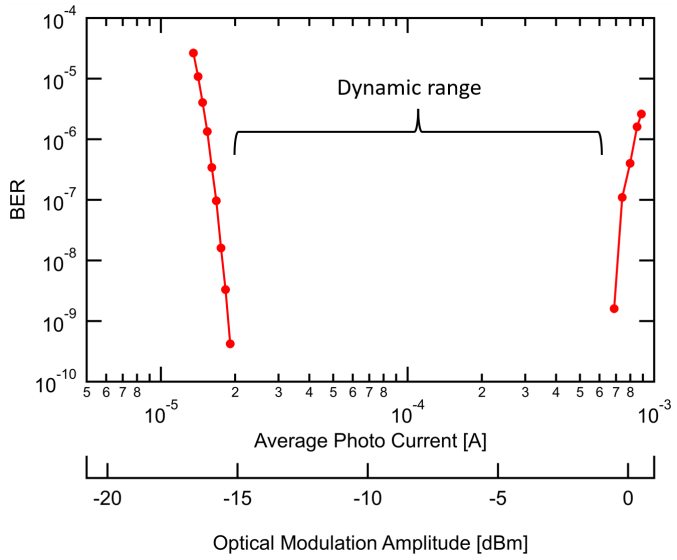

Figure 1: Example dynamic range of a VTRx+ receiver measured with PRBS23 test pattern.

Strong saturation, as shown on the right handside of the bathtub curve, would be observed as increased error rate in the downlink. However, it's important to note that this problem is likely to manifest first in the uplink before any observable performance degradation occurs in the downlink due to saturation. This is due to the fact lpGBT, when operated in transceiver mode, recovers the clock from the incoming data stream. VTRx+ receiver saturation causes increased deterministic jitter in the electrical signal used in this clock recovery, Fig. 2. As the uplink data rate is four times higher than that of the downlink, it is more sensitive to increased jitter.

Saturation is strongly dependent on three factors: input optical modulation amplitude, as shown above, receiver supply voltage, and used pattern lengths. Examples of these dependencies are shown in Fig. 3 where time interval error (TIE) histograms are presented. With short pattern lengths saturation does not occur even with the highest measured optical input powers and lowest used receiver supply voltages, see top right corner of Fig. 3. With a longer patter the dependence to both supply voltage and input optical modulation power becomes evident, PRBS15 in the middle row, and the situation gets even worse when the pattern length is increased to PRBS31, bottom row.

The pattern dependence is caused by the saturation process that requires an increase in the running disparity of the bit stream. If the pattern length is short, e.g. PRBS7, running disparity never reaches the required level, but in case of a longer pattern lengths the probability of few long sequences of ones or a large number of shorter sequences of ones dominating over bits at zero state becomes higher and higher. This also means that one extremely long sequence of ones is not necessarily required to trigger large jump in TIE. Two examples to illustrate this process are shown in Figures 4 and 5, the first of which demonstrate how a increased TIE occurs even though only relatively short consecutive sequences of ones is present, and the second illustrates how one long sequence can trigger a dramatic increase in TIE.

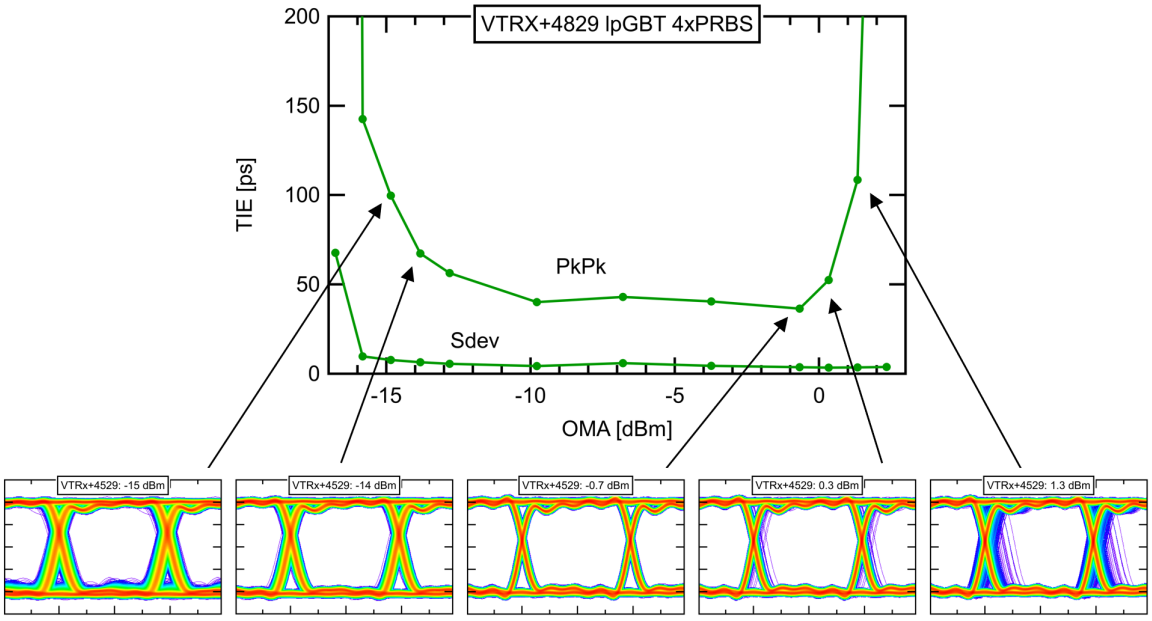

Figure 2: At high input optical modulation amplitudes deterministic jitter in the VTRx+ receiver's electrical output increases strongly with increasing input amplitude.

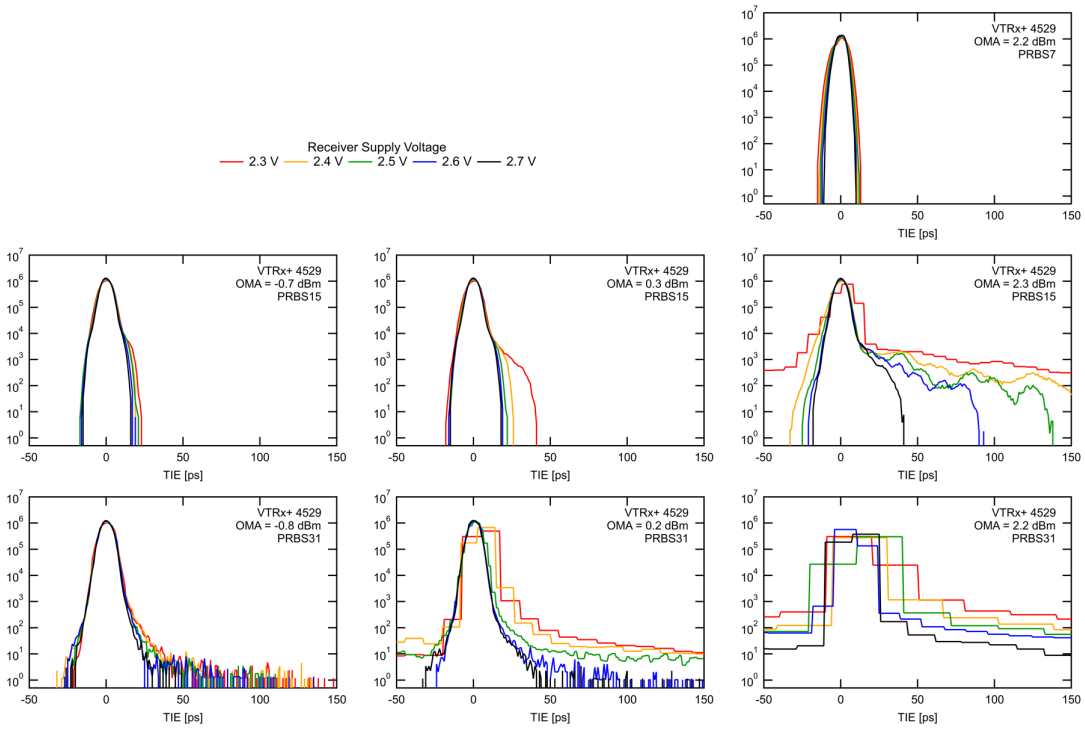

Figure 3: Time interval error histograms captured from the VTRx+ receiver's electrical output with different receiver supply voltages (colors), increasing input optical modulation amplitude (from left to right), and increasing pattern length (from top to bottom).

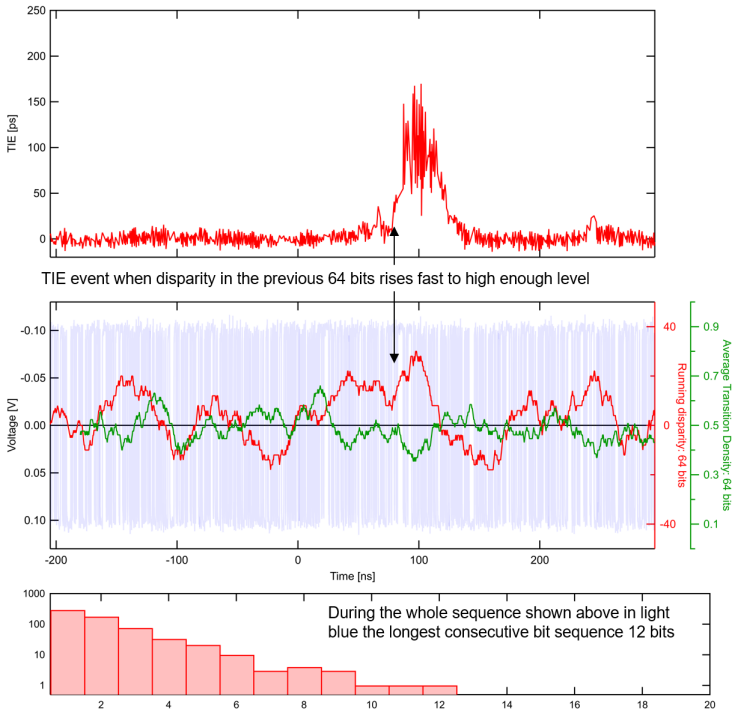

Figure 4: Example of an TIE event during which the longest sequence of ones was only 12 bits (histogram on the bottom), but to trigger the event (graph on the top) the running disparity (red trace in the middle) had to increase significantly. During the whole capture the average transition density (green trace in the middle) did not experience anything significant.

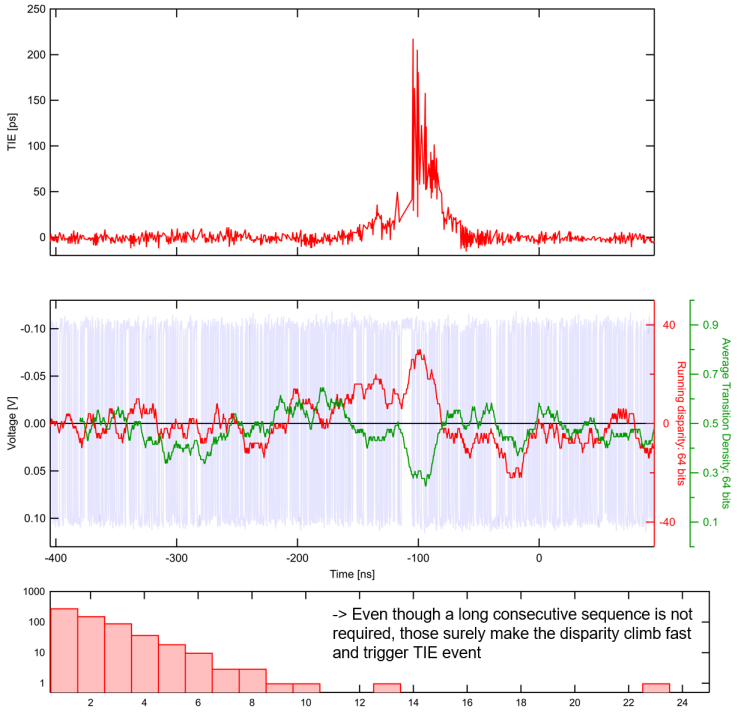

Figure 5: Example TIE event which after some initial increase in the running disparity is finally triggered by long sequence of 23 consecutive bits at one state.

Mitigation

As shown above there are three main factors that cause the receiver saturation. In order to mitigate the issue at least one of these factors must be improved sufficiently. Firstly, the users should ensure that the VTRx+ transceivers are operated with nominal receiver supply voltages, because while receivers can operate with much lower supply voltage than specified it will emphasize the saturation problem.
Secondly, the saturation becomes non-issue if the pattern lengths are kept short enough. However, as VTRx+ transceivers are typically used in combination with lpGBT and running its data protocol, it is not possible to change the scrambling and interleaving that happens in lpGBT. Unfortunately, lpGBT scrambling is not quite powerful enough to ensure that saturation would not happen in the VTRx+ receiver.
Therefore, the third and final mitigation method is likely the only practical for the users: if the input optical modulation amplitude is reduced enough the saturation wont cause degradation in the receiver performance. This reduction in the OMA can be achieved in two ways: the users who do not have access to the back-end Samtec FireFly trancseivers' I2C monitoring and control registers can use physical inline attenuators. These attenuators are available in different attenuations and in different configurations in terms of attenuated and non-attenuated channels.
If the user can access the I2C control, the bias and modulation settings in the FireFly transceivers can be tuned. Fig. 6 shows the effect of the FireFly bias and modulation tuning on the VTRx+ receiver output jitter. The graph on top left shows the total jitter, which increases with high modulation settings and with high extinction ratio signals. The former is caused by increase in the deterministic jitter (bottom left) and especially its periodic jitter contribution (bottom right). The latter is caused by increased random jitter with high extinction ratio modulation. Therfore, the optimal direction of the settings tuning is to reduce both bias and modulation settings from the defaults (around the red marker) as indicated with the yellow arrows. It is recommended to reduce the settings in sequence and observe the changes in the uplink link errors after each settings change, to avoid unnecessarily large change in the input optical modulation amplitude and reduced sensitivity margin.

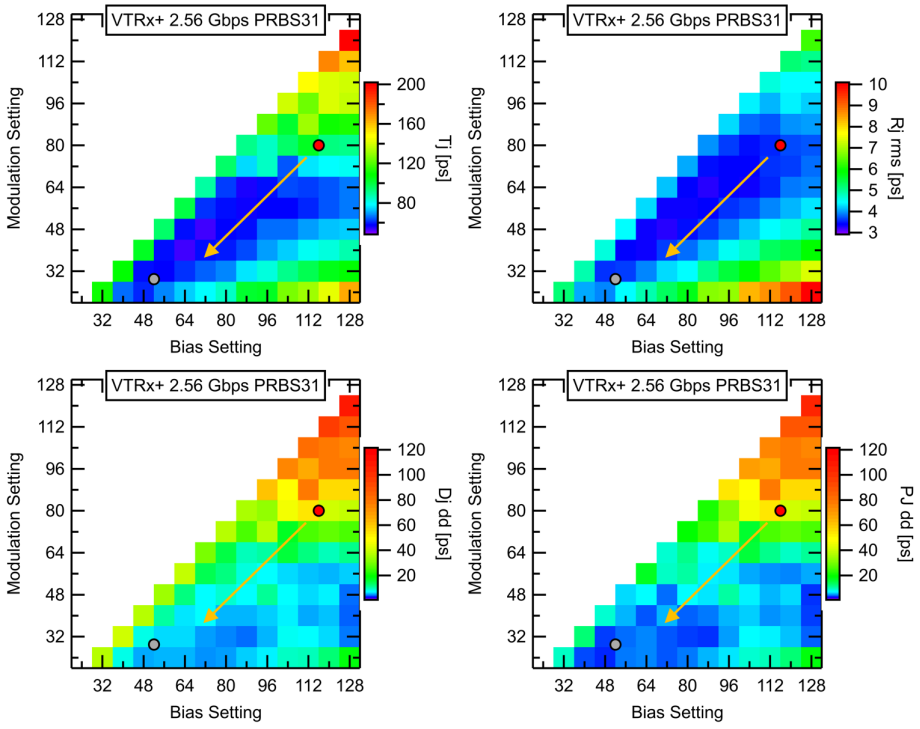

Figure 6: Example how changing Samtec FireFly bias and modulation settings effect the jitter in the electrical output of a VTRx+ receiver. Excessive deterministic jitter (Dj and Pj on bottom) causes a region of high total jitter (top left) when high modulation settings are used.

Recipe for Samtec FireFly settings optimization

Whether receiver saturation is present, and to what extent, depends on device-to-device variations in both Samtec FireFly transmitters and VTRx+ receivers, as well as the fiber plant. Therefore, it is recommended to optimize the FireFly settings only when necessary and by reducing the bias and modulation settings in a step-wise manner. This ensures that the link's sensitivity margin is not unnecessarily reduced. This step-wise optimization routine has to be done only for one time. Once the optimized settings are found, they can be saved to a lookup table and set directly after power-on in the future. Note that the settings change is not permanent and FireFly transmitters reset back to the default settings when powered on.
The default settings in the high-power CERN-B FireFly transceivers are around 116 (bias) and 80 (mod), and the user can tune the settings using the following procedure. It is recommended to observe link performance after each step, starting with the settings shown at (a) and continuing with the following steps (b to e) only if the performance is not sufficiently improved. One method to monitor the effectiveness of the settings change is to observe corrected uplink errors. This can be done, for example, if an uplink FEC flag monitoring is implemented with the lpGBT-FPGA IP core on the back-end as in the lpgbt-fpga-kcu105 example design (`upLinkFECCorrectedLatched_s`). The FEC flag should be reset (`upLinkFECCorrectedClear_s`) after a settings change, after which it indicates whether corrected errors are still present, see https://lpgbt-fpga.web.cern.ch/doc/html/index.html and https://gitlab.cern.ch/gbt-fpga/lpgbt-fpga-kcu105.
Recommended Bias and modulation settings steps:

(a) Bias 112 (0x70), modulation 72 (0x48)

(b) Bias 104 (0x68), modulation 64 (0x40)

(c) Bias 96 (0x60), modulation 56 (0x38)

(d) Bias 88 (0x58), modulation 48 (0x30)

(e) Bias 80 (0x50), modulation 40 (0x28)

Bias and modulation settings can be changed with the following process:

- Access so called "Block mode":
  1. Set module address to `0x50`:
     `0x00, W, 0x43 0x50`
  2. Ensure that the page is `0x00`:
     `0x50, W, 0x7F 0x00`
  3. Set password to "GOBL":
     `0x50, W, 0x7B 0x47 0x4F 0x42 0x4C`
  4. Change page to `0xCE`:
     `0x50, W, 0x7F 0xCE`
  5. Write dummy data to register `0x80`:
     `0x50, W, 0x80 0x00`
- Make adjustments (cc = channel, 0 based). Steps 6 and 7 can be repeated in order to find good settings, as explained above and with the settings shown in (a) to (e):
  6. Set laser bias:
     `0x50, W, 0x49 cc bias`
     e.g. `0x50, W, 0x49 0x00 0x70`
  7. Set laser modulation:
     `0x50, W, 0x4A cc modulation`
     e.g. `0x50, W, 0x4A 0x00 0x48`
- After optimized settings have been found:
  8. Set command back to memory map mode:
     `0x50, W, 0x6A`