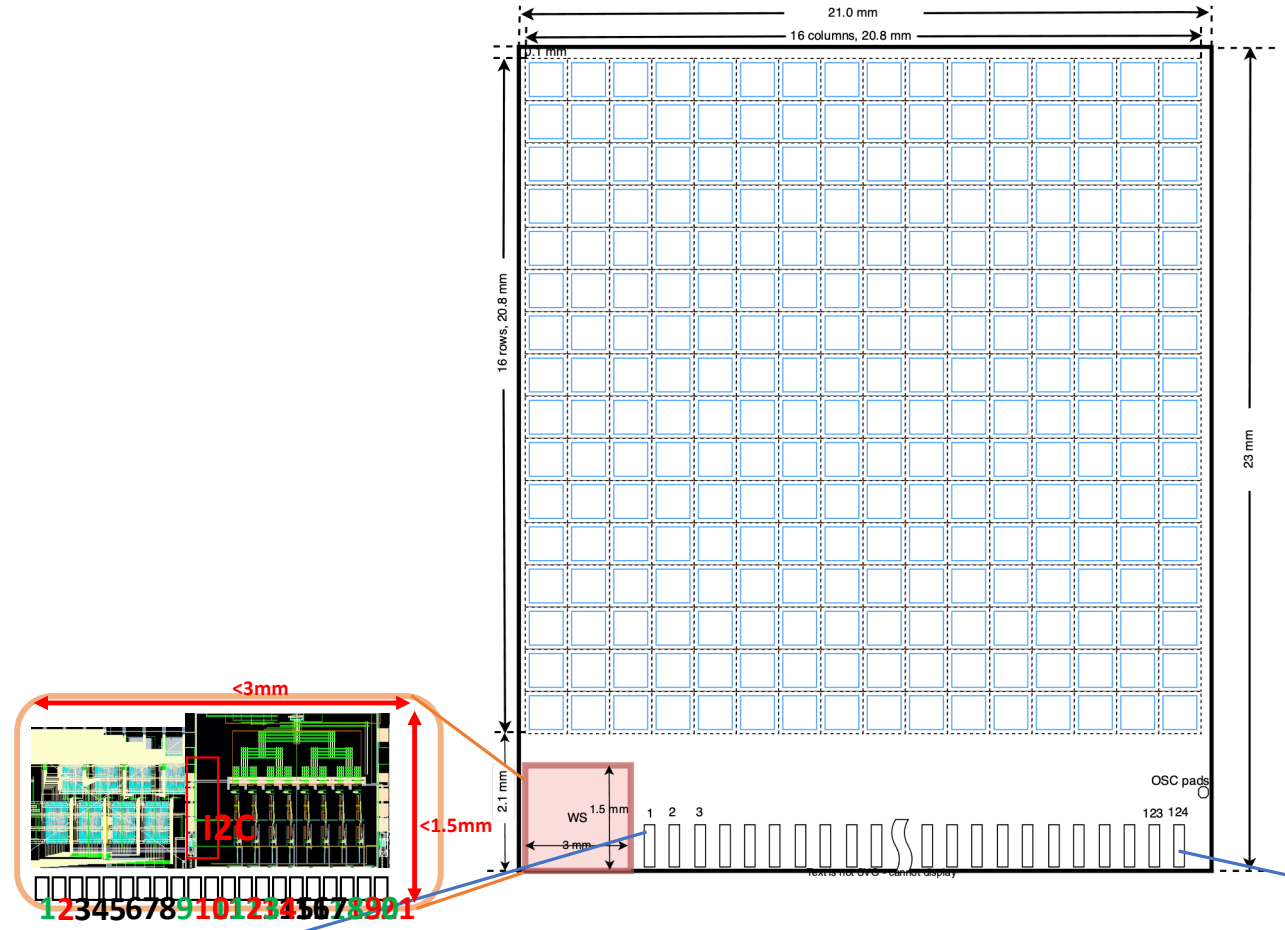
ETROC2 questions and answers (FAQs)
→ questions from Andrew

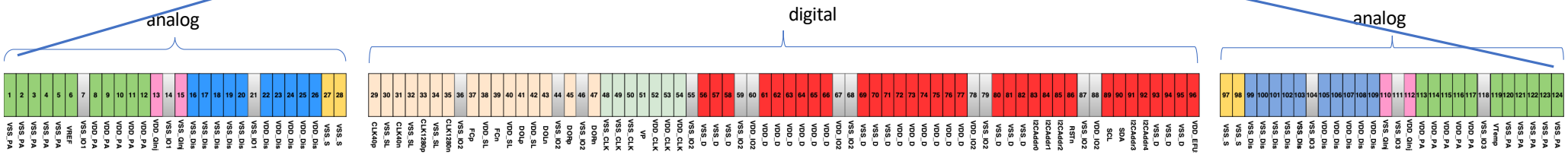
Quan Sun and Ted Liu for the ETROC team

updated on June 13, 2022



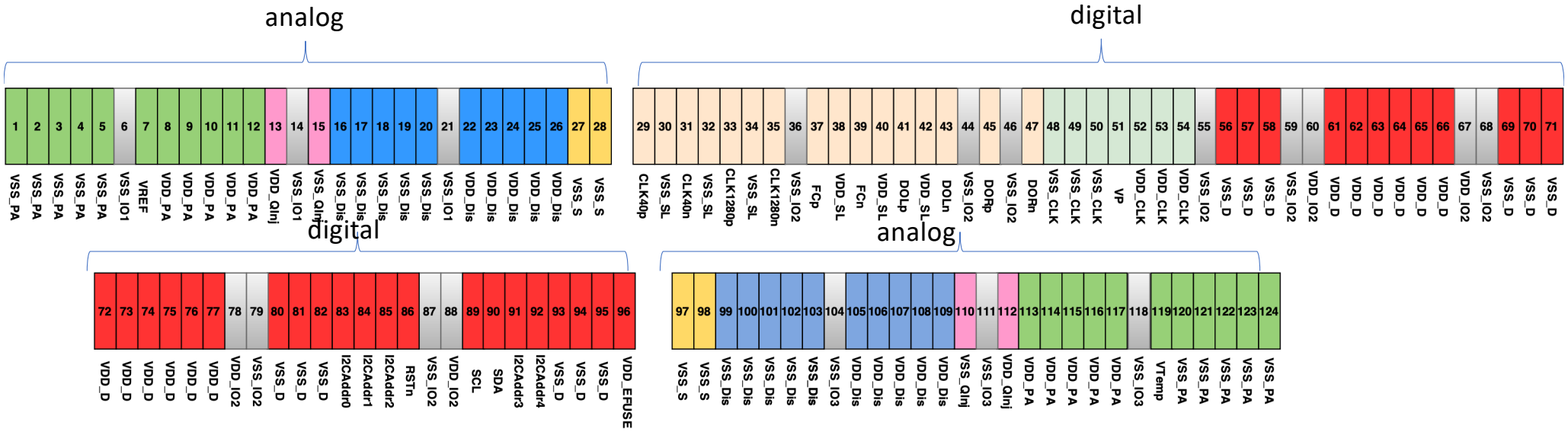
New pinouts update by Quan on June 7th, 2022

- Tentative chip size: 21.0 X 23.0 mm^2
- Tentative pads information excluding waveform sampler
  - Pad number: 124
  - Pad opening: 70 X 200 um^2
  - Pad pitch: 143 um
  - Edge-to-edge space: 73 um
  - one probe pad on the bottom right for probing an on-chip ring oscillator output.



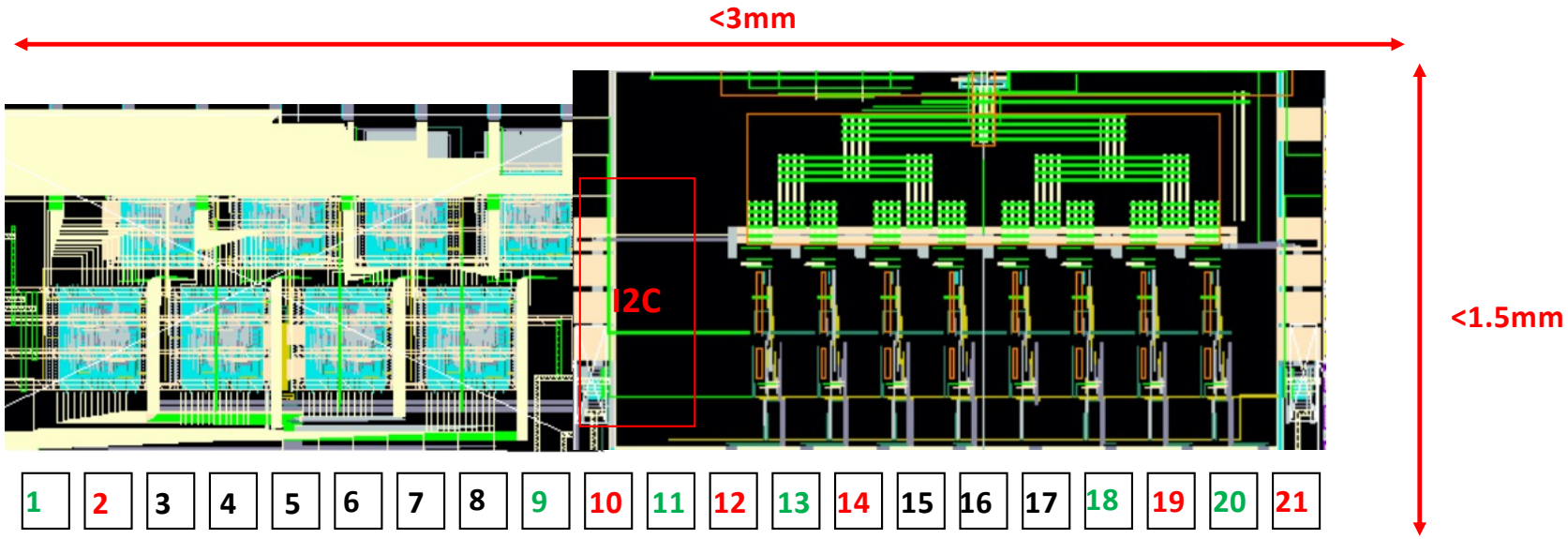
- A couple of power domains on the chip: PA, Discriminator, Charge Injection, Serial link, CLK, Digital/TDC
- Two power domains(analog/digital) on the board

- VSS_IO pads in analog domain connected to a common ground for ESD protection.
- VSS_S is the substrate connection
- Ground pads in a power domain are grouped together
- Supply pads in a power domain are grouped together

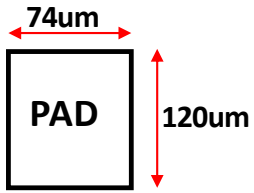


New pinouts update by Quan on June 7th, 2022

WS Floorplan for ETROC2



- WS will be placed at the bottom left corner of ETROC2 chip
- Power Pads are marked in red; Ground Pads are marked in green
- Pad dimension: 74 (horizontal) x120 (vertical); Opening: 70x116
- Pad pitch 130



Waveform sampler is integrated in the ETROC2 (initial integration done).
An updated ETROC2 pinouts excel file including waveform sampler pads will be sent via email.

WS PAD Description

Pad #	name	Type	Description	Typical Value
1	DVSS	Digital ground	Digital ground	0V
2	DVDD	Digital power	Digital power	1.2V
3-7	I2C_addr<4:0> (Pad#3 for MSB)	I2C address pads	I2C address	N/A
8	wr_en	Digital input	External write enable signal	N/A
9	DVSS	Digital ground	Digital ground	0V
10	DVDD	Digital power	Digital power	1.2V
11	AVSS	Analog ground	Analog ground	0V
12	AVDD	Analog power	Analog power	1.2V
13	AVSS	Analog ground	Analog ground	0V
14	AVDD	Analog power	Analog power	1.2V
15	SCL	I2C pads	I2C pads	N/A
16	SDA	I2C pads	I2C pads	N/A
17	RSTN	I2C pads	I2C pads	N/A
18	AVSS	Analog ground	Analog ground	0V
19	AVDD	Analog power	Analog power	1.2V
20	AVSS	Analog ground	Analog ground	0V
21	AVDD	Analog power	Analog power	1.2V

FAQ: (questions from Andrew)

1. VREF: does this need to be connected to the RB? If so, as an input or output? I understand that it can function as both, possibly for diagnostic purposes, but we need to know it needs to be connected on the RB (if at all).

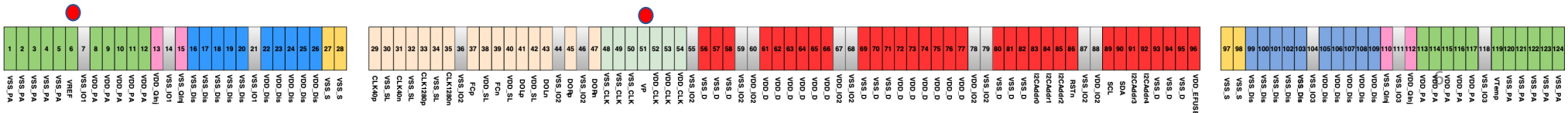
VREF: this is a reference voltage used by DAC (directly related to the discriminator threshold) and charge injection. It is generated inside the chip, with the option that can be provided/applied externally (this option is for testing purpose only). By default, it is used for monitoring purpose.

On the ETROC2 chip test board, VREF is output for diagnostic purposes or input in case the internal VREF generator doesn't work (for testing purpose only).

In the system (module and readout board design), it is recommended to monitor VREF with an ADC as it is directly related to discriminator threshold.

2. VP: Do you have any recommendation for the capacitance (or possible range of capacitances)?

This is meant for stabilizing the PLL VCO (voltage controlled oscillator) power supply. A 0.1 uF capacitor is recommended for VP. This is optional. We recommend to have this option for the first round of prototype design and will test to see if we really need it or not (floating vs 0.1uF).



FAQ:

3. CLK1280P/N: can you confirm whether this can be left floating?

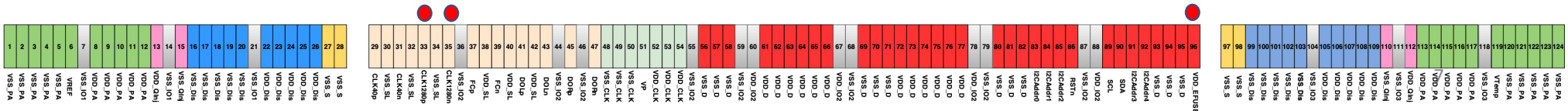
This is 1.28 GHz optional clock input for testing and performance study purpose only. Not required for module design, and CLK1280P/N can be left floating if not being used.

4. VDD_EFUSE: does this need to be connected on module or can it be left floating?

This is the 2.5V supply for EFUSE programing.

Should leave it floating in the final system as we plan to program EFUSE during wafer probing testing stage.

For the first module/readout board design, if feasible, consider using it only if one wants to program the EFUSE to keep track of the chips (note: the initial diced ETROC2 chips will not have the EFUSE programed). The ETROC2 test board will use it for sure.



FAQ:

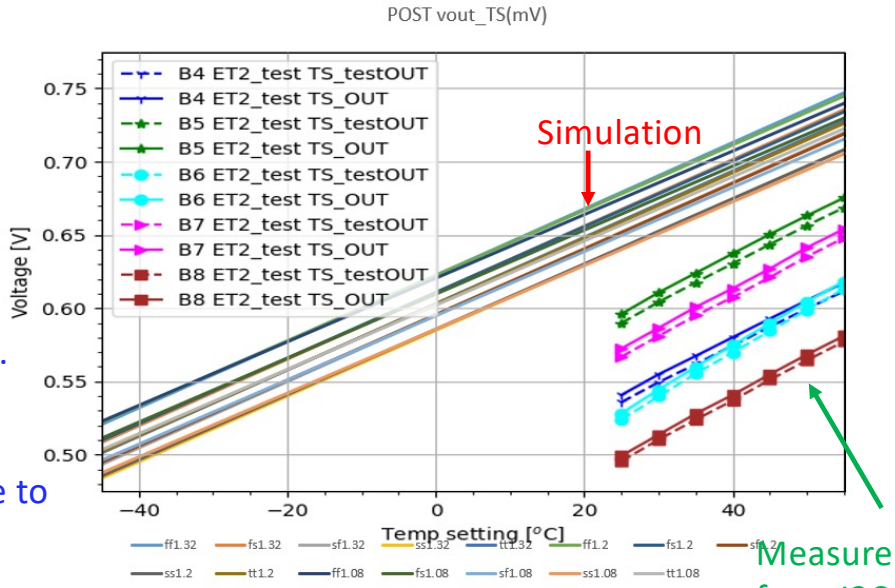
5. VTemp: Can you please specify some details about this signal? e.g. What is the voltage range?

This is the output of the build-in Temp Sensor on ETROC2.

The plot shows the VTemp vs temperature in simulations and measurements from ETROC I2C test chips. The measured curves from test chips are offset down from 50mV to 150 mV, but the sensitivity (delta VTemp/ delta temperature ~ 2mV/degree in C) is close to what predicted by the simulations.

The chip-to-chip variation of the sensitivity is small enough for the purpose of monitoring temperature changes.

The expected voltage range is approximately from 300 mV to 700 mV(over temperature from -40 to 50C, including chip process variation).



Measurements from I2C test chips

FAQ:

6. As you know, AVDD and DVDD will be from a common supply. Can we simply treat them as one net or is any kind of filtering required for any of the analog supplies?

If feasible, it is recommended to isolate AVDD and DVDD with ferrite bead.

(need more discussions here, related to power board design as well. Keep in mind that ETROC uses lpGBT PLL).

7. Can waveform sampler AVDD / DVDD be treated as a single net along with the ETROC voltage or must the AVDD be filtered in some way? (same question as above for the ETROC)

Based on most recent testing on Rad-hard waveform sampler chips, the AVDD and DVDD are treated as a single net on the testing board (using ideal power supply at lab).

8. Do you have any simulations/recommendations for power supply decoupling?

We don't have detailed simulation. We would recommend some 0.1uF ceramic capacitors placed very close to the ETROC. Besides that, we expect some capacitors(10 uF) for DC/DC power supply filtering on the readout board close to the connector to the module.

FAQ:

9. Do the ADDR inputs have built-in pull-ups or pull-downs?

Yes, there are 40 kOHM internal pull-down resistance on these input.

10. Does the RESET input have built-in pull-up or pull-down?

Yes, there is 40 KHM pull-up resistor for Reset input.

FAQ:

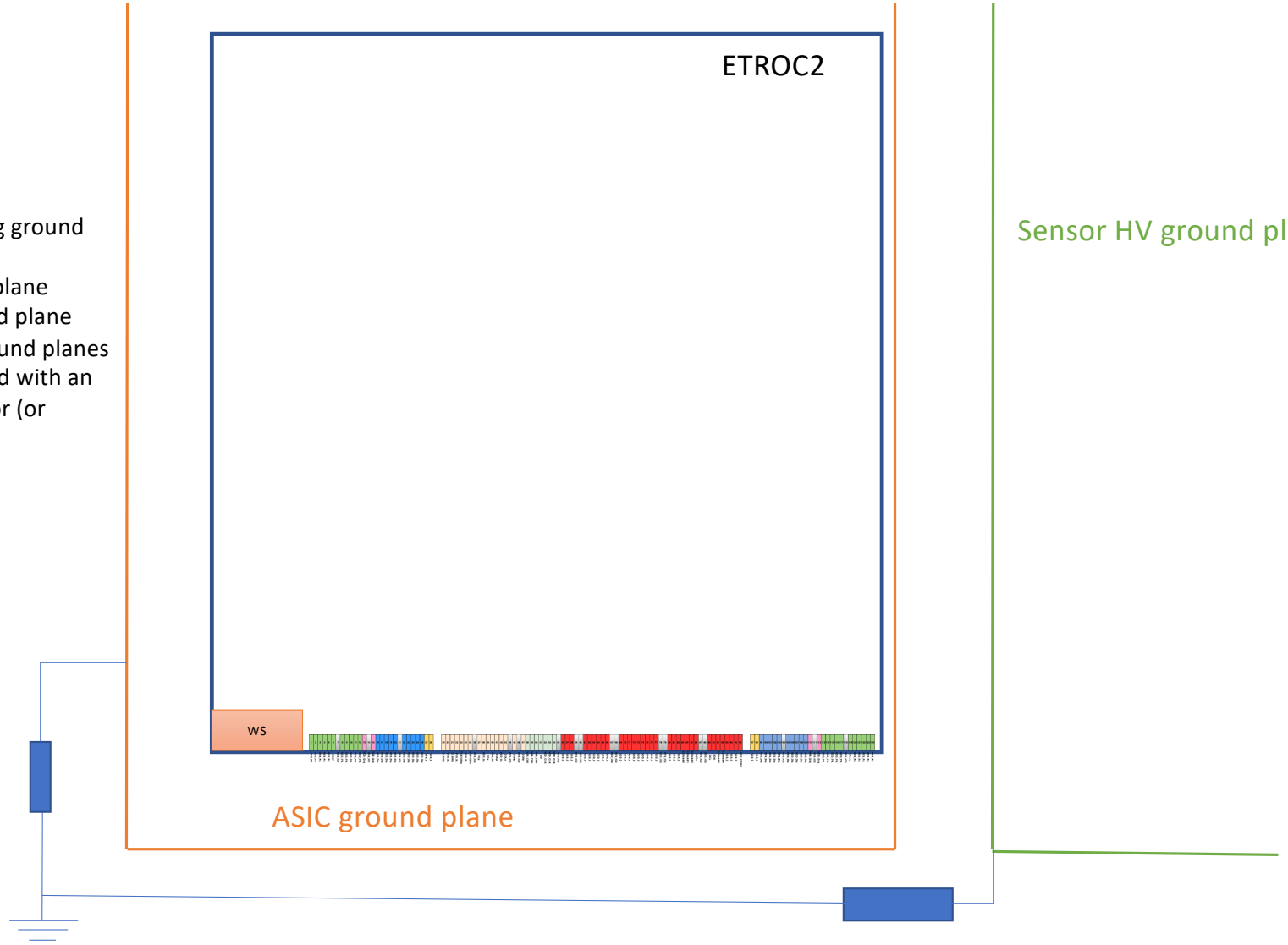
11. Since this presentation[1], do you have any update on a preferred ground scheme? (AGND/DGND vs. ASIC GND / HV GND)?

[1] https://indico.cern.ch/event/1139028/contributions/4779384/attachments/2406930/4117689/ETROC2_Pinout_v2%20-%20Read-Only.pdf

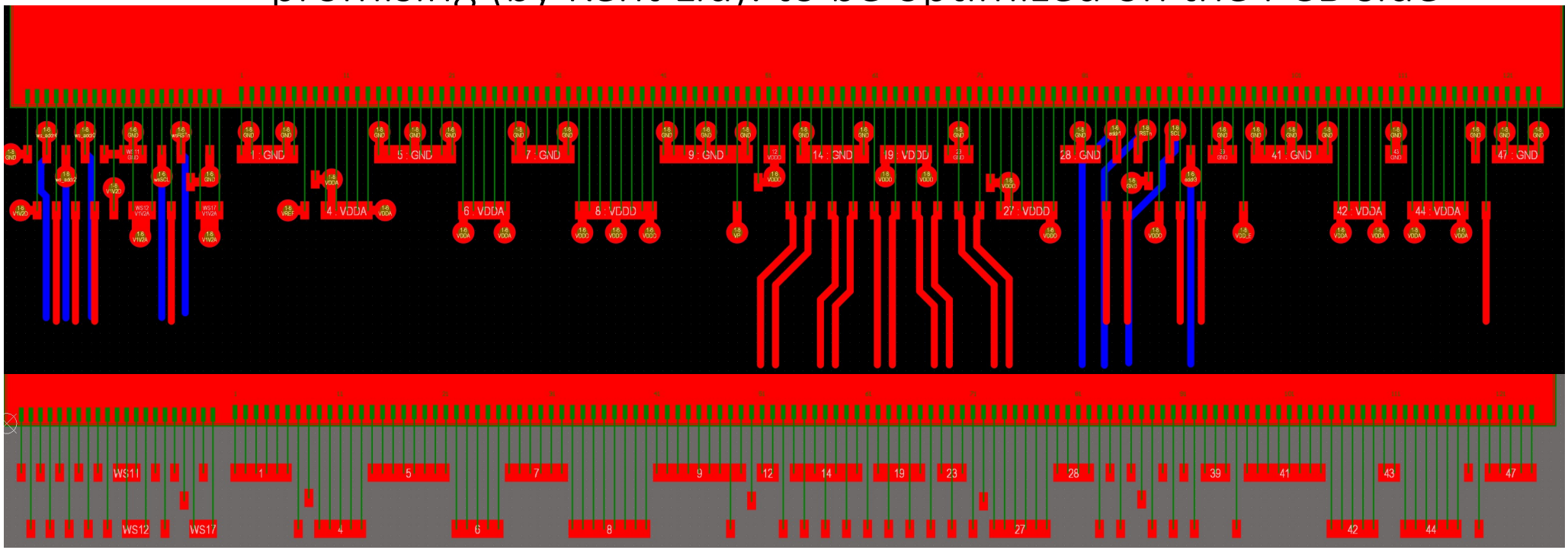
See next few slides

Updated Possible PCB ground scheme

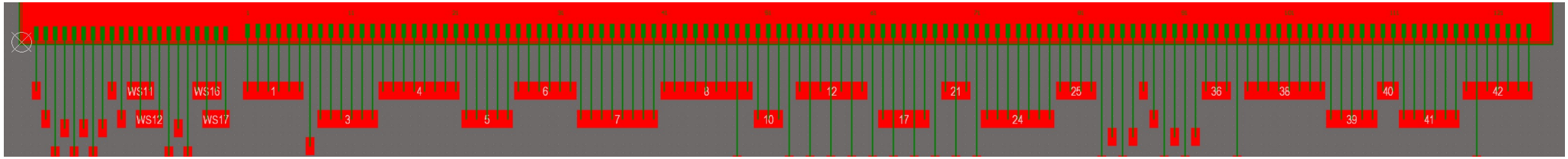
- Two nonoverlapping ground planes on the PCB
  - ASIC ground plane
  - Sensor ground plane
- Connecting two ground planes to a common ground with an inductor or a resistor (or multiple)



Initial ETROC2 test board bonding diagram exercise looks promising (by Kent Liu): to be optimized on the PCB side

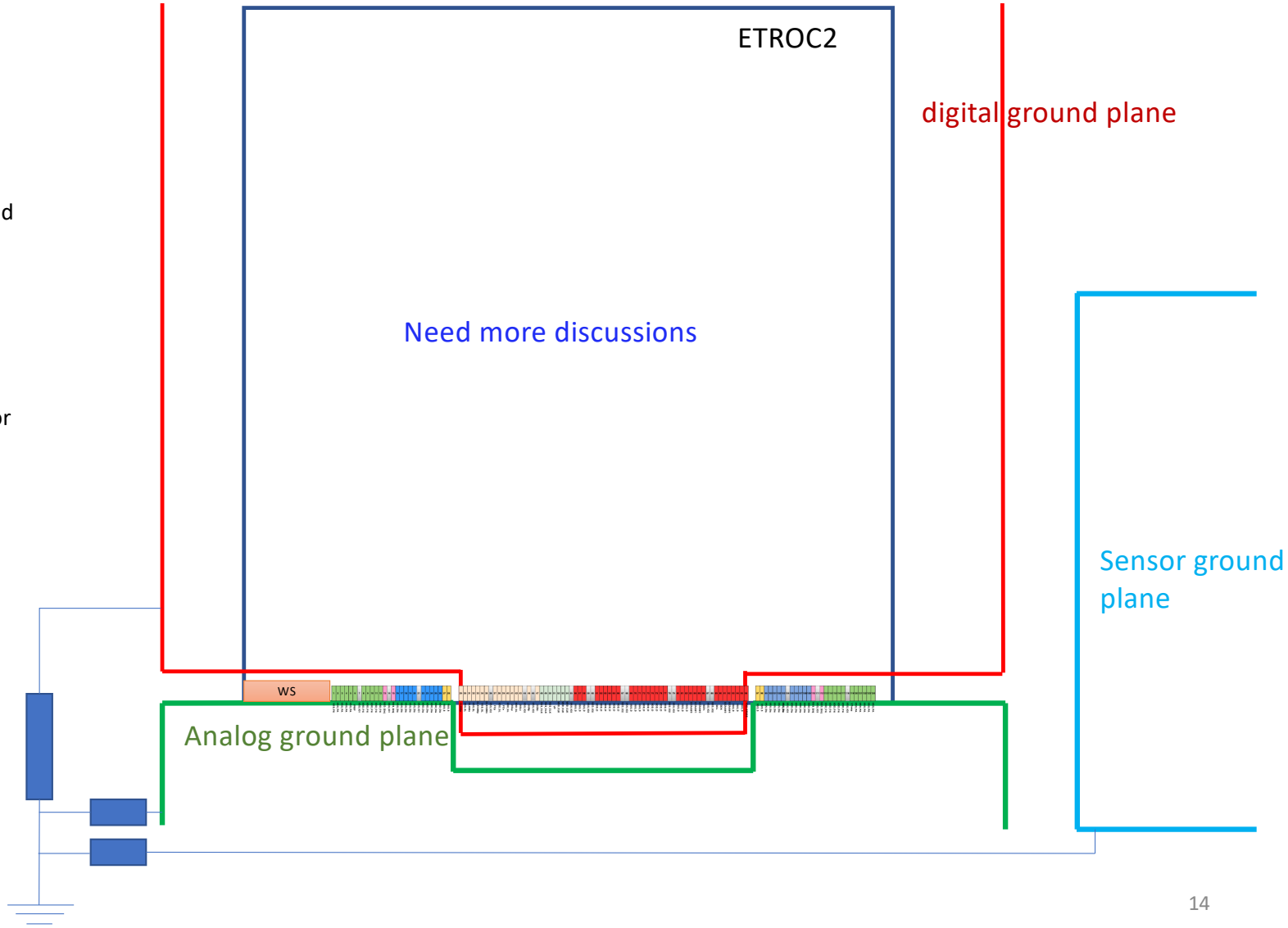


Second round of optimization: assume Option One (to be updated)



Updated Possible PCB ground scheme

- Three nonoverlapping ground planes on the PCB
  - digital ground plane
  - Sensor ground plane
  - Analog ground plane
- Connecting three ground planes to a common ground with inductors or resistors (or multiple)



FAQ:

12. Can the waveform sampler be on the same I2C bus as the ETROC? What is the base I2C address of the waveform sampler and the ETROC?

There are 5-bits I2C address for WS and ETROC, and each can be set separately by user on test board or module. There are 2-bit internal I2C address. For main ETROC2, the 2-bits will be set as 11 internally (two MSB). For WS, the 2-bits will be set as 01 internally (two MSB).

13. Do the waveform sampler I2C pins have integrated pull-ups / pull-downs?

For ETROC2 waveform sampler, the I2C pins do not have integrated pull-ups/downs.

for ETROC3, the plan is to have the I2C for WS integrated with the main ETROC.

14. What is the WR_EN pin of the waveform sampler and what (if anything) should it be connected to?

wr_en: External write enable signal for the memory (Can be used to test WS without involving fast commands). This is for testing purpose only. No need to connect to it for module design.

15. Does the RSTN of the waveform sampler have integrated pull-up / pull-down? Can it be bonded to the same reset as the ETROC or should they be connected to separate lpgbt / sca GPIO?

The I2C RSTN pad has integrated pull-up (the earlier slide labeled it as RST, should be RSTN). For ETROC2, it is recommended to keep the reset separate for the main ETROC2 and the waveform sampler.

FAQ:

12. does the 40MHz clock input have internal termination or does it need an external 100 ohm resistor?

Each of these serial inputs(40 MHz clock/Fast command/1.28 GHz clock) has optional internal termination which can be enabled or disabled with I2C.

But the internal termination resistors have tolerance of about +-20%.

Users can choose to use the internal termination or put an external termination on the board with better tolerance.

Suggestion: if feasible, for the first prototype, it is better to include an external termination for testing purpose (to compare with using internal termination).

13. And same question for the Fast command port.. I know it is multi-drop on our module but I'm not sure if that needs to be done with external resistors or by I2C configuration.

For fast command, the multi-drop is two stage, only the second one needs termination. One could simply use I2C to enable the second one (and disable the first one).

But if you have room, you can also put an external termination on the second one for testing purpose. If turns out the external termination and internal termination all work the same,

then later you can remove the external termination for the next version.

14. Does the downlink on the ETROC support polarity inversion, or must the P and N sides of the diff pair be assigned correctly?

Yes, ETROC supports it.

15. Do you have any approximate breakdown of the power consumed by the analog and digital domains separately? I have seen total power estimates but wondering how that breaks down, e.g. 0.25W analog 0.75W digital or whatever the real number is.

we know most the measured power consumption for almost all (if not all) of the analog blocks from test chips. For the digital, we had some estimate, but chance is good that the actual could be lower than the estimate due to extensive optimization. But we wouldn't know for sure until more detailed power analysis is done after full chip integration is finalized.... I presented the details of the breakdowns (an update of power consumption of ETROC) a while back, need to find that talk at ETL Front-end meeting (sometime last year). Also need to include the waveform sampler (only enabled for a short period once in a while).

See slides next.

ETROC power consumption measurements

ETROC0/ETROC1 testing results

Final ETROC0/1 design simulation results

Table from TDR

Circuit component	Power per channel [mW]		Power per ASIC [mW]	
Preamplifier (low-setting)	0.67	0.76 0.74	171.5	189.4 (preamp low power)
Preamplifier (high-setting)	1.25	1.31 1.27	320	325.1 (389.1, the highest power)
Discriminator	0.71	0.87 0.84	181.8	215.0
TDC	0.2	0.07 0.1	51.2	25.6
SRAM (→ memory)	0.35	0.25 (sim)	89.6	64.0
Supporting circuitry	0.2	0.2 (reserve)	51.2	51.2
Global circuitry			200 →	234.5

- Measurements agree with simulation of ETROC0 and 1 design
  - TT corner numbers shown, mostly agree reasonably well
  - ***But should assume up to 20% variation with real production***
  - Note: preamp highest setting (4th gear) power is 1.52mW (measured), the high-setting above is the 3rd gear.

Sum: ~780/915/980 mW (low/high/highest power)
Use 980mW & add 20% for worst case.
(***to be confirmed by ETROC2 measurements***)

- The new 0.25mW SRAM is based on estimate by expert (ETROC2 will not use SRAM, power is expected to be lower)
- The "supporting circuitry": reserved for circuitry hard to be separated clearly
- The "global circuitry" (a guess back then for TDR, with large uncertainty)
  - ***A lot is known now about global circuitry blocks (ETROC2 simulation)***
    - ***PLL: 60mW; Phase shifter: 2 mW; Clock distribution: 25mW;***
    - ***Tx: 16mW; Rx 1mW. Fast command decoder: 2mW***
    - ***Voltage reference generator: 0.5mW.***
    - ***Readout: 100mW (guess so far); other misc: 20mW (guess)***

106.5
+
120
+ 8
= 234.5 mW

- ***Waveform sampler: when disabled, ~8mW (negligible)***
  - ***When fully enabled (for a short period, sub ms or micro-second): 141mW***
  - ***This means momentarily, the power could reach 1100mW when WS is enabled.***

Power Consumption

ADC EN	Input Buffer and On-chip Bias
1	16mW
0	3mW

VGA EN	ADC EN (Including clk gen)	Analog Power (VGA+ADC)
1	1	105mW
0	1	87mW
0	0	5mW

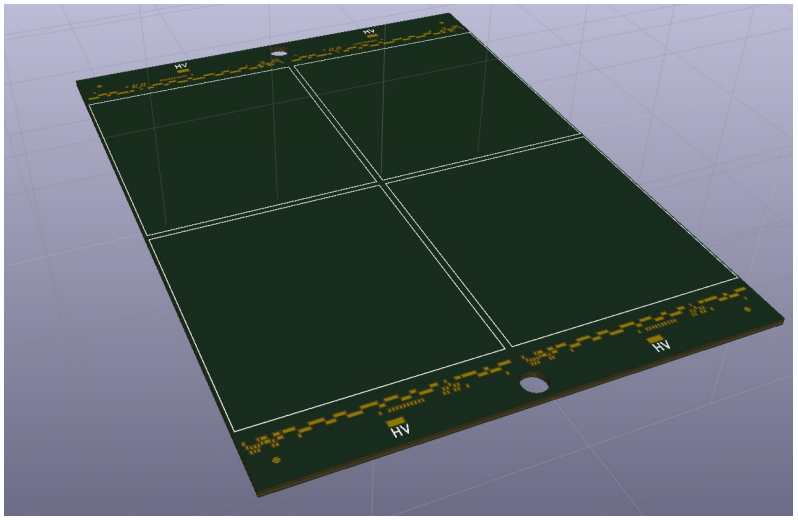
WR EN	RD EN	ADC EN	Digital Power
1	0	1	12mW
0	1	1	11mW
0	0	1	9mW
0	0	0	~0mW

On ETROC2:
Delivering 2.56GHz clock to WS: ~20mW
(when not in use, this clock is disabled)

When WS disabled: ~ 8 mW

When WS is fully enabled (for short period, sub ms): 141mW. For module/readout board/power design, keep this in mind.

Email from Caleb



I had a chance to try out the proposed bond pad pattern with the ETROC2 module design. Overall, I don't see any show-stoppers. I've attached the gerber files with the updated design.

I have a few comments that I'll list below:

1. The shortest wirebonds are shorter than what we believe are feasible for all of the wirebonders at the module factories. I pushed them out to about 1.4mm (this is reasonable)
2. Based on a suggestion from Daniel, I replaced the 4 mounting holes located in the corners with just 2 that are centered along the short edge of the module.
3. Because of the change in the mounting holes, there is now a hole where the HV bond pads were located. To deal with this, I added a HV bond pad for each sensor (going from 2 previously to 4 pads now). This implies that there will also be 4 cutouts in the baseplate instead of 2, and the HV bonds will be attached on the sensor edge, rather than the corner. (for the first design, perhaps make the HV pad longer)
4. The new placement of the HV bonds will require further investigation to make sure that there is no risk of sparking between the HV bonds and the ETROC bonds. This could potentially be an issue since the HV bonds need to arch over the lower-profile ETROC bonds to reach the sensor.

One minor thing to remind people:

Dimensions ETROC & Sensor as of 8 Feb 2022

Final design:

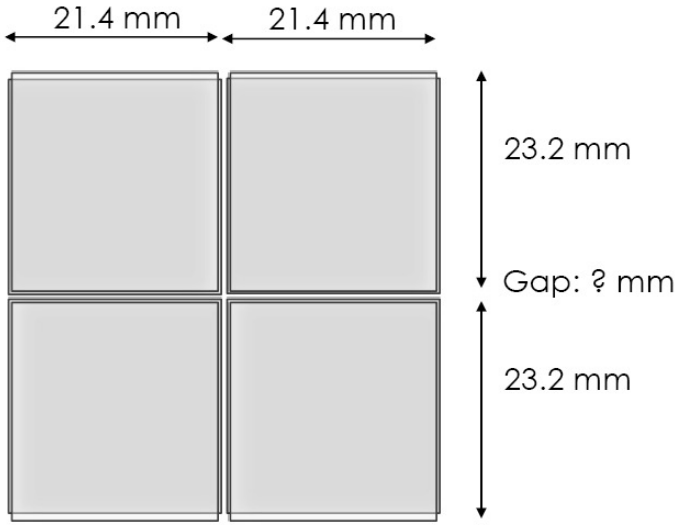
Sensor: 21.4 x 21.6 mm^2 (proposed)

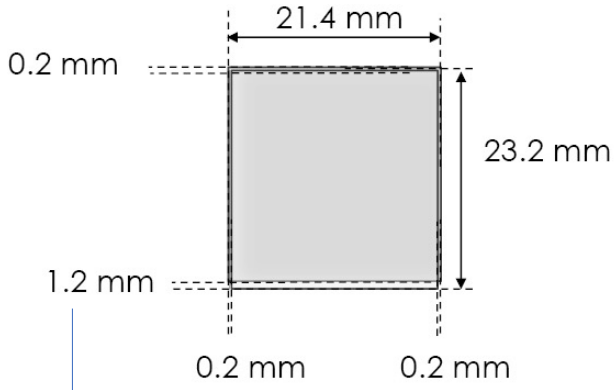
ETROC: 21.0 x 23.0 mm^2

Combined: 21.4 x 23.2 mm^2
(shall we call it "assembly"?)

Total thickness: not defined

Dimensions summarized by Nicolo in Feb.





This should be 1.6mm based on ETROC2 and sensor dimensions (checked with Nicolo)
(this was noticed by Sergey Los recently during a discussion)