FERMILAB-TM-2746-CMS-E

ETROC1 Design Note

Abstract: This document provides the relevant information needed during ETROC1 design integration stage, and it is now improved to be used as a guide for testing ETROC1 prototype chips.

Version 1.1, November 7, 2020

Christopher Edwards[a], Datao Gong[b], Xing Huang[b], Kent Liu[b], Tiankuan Liu[b], Ted Liu[a], Sandeep Miryala[c], Jamieson Olsen[a], Hanhan Sun[b], Quan Sun[a], Jinyuan Wu[a], Jingbo Ye[b], Li Zhang[b], Wei Zhang[b]

[a]Fermi National Accelerator Laboratory, Batavia, IL, USA

[b]Southern Methodist University, Dallas, TX, USA

[c]Brookhaven National Laboratory, Upton, NY, USA

Technical contact: Quan Sun, qsun@fnal.gov

Project contact: Ted Liu, thliu@fnal.gov

Table of Contents

1 ETROC1 OVERVIEW

ETROC1 is the second prototype of ETROCn (ETL readout ASIC chip). It is developed with TSMC 65 nm CMOS process (CMN65, RF) and the metallization option is 1p9m-6x1z1u.

ETROC1 aims to demonstrate full chain frontend, including the preamp, the discriminator and the TDC, and a 4 X 4 array. It interfaces with a 5 X 5 sensor with pixel size of 1.3 X 1.3 mm^2, which is similar to ALTIROC1. 17 (16 for the array and 1 for the standalone test block) out of the 25 pixels are to be connected to the readout circuits and other 8 pixels are dummies. Signal pads of dummy pixels are pulled down.

The tape-out date is Aug. 28, 2019, and turnaround is about 10 weeks.

2 ETROC1 STRUCTURES

2.1 BLOCK DIAGRAM

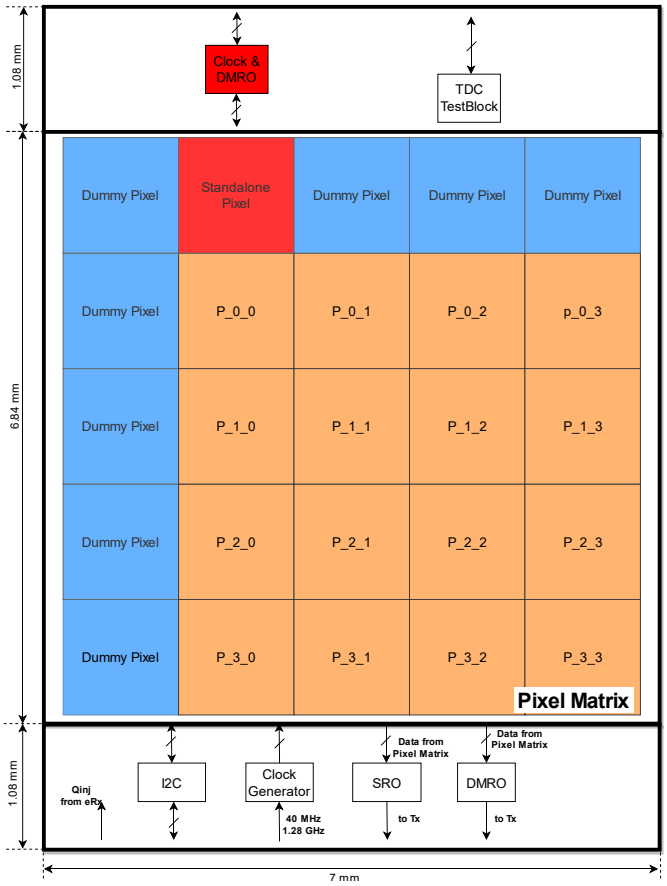

Figure 2.1.1 Block Diagram of ETROC1

2.2 CLOCK GENERATION SCHEME

The baseline clock generation scheme is receiving an off-chip 1.28 GHz clock, generating the phase-shifted 40 MHz and 320 MHz clocks with the divider and the phase shifter. The TDC pulse generator generates pulses for the TDC and for off-chip checking. An optional scheme is directly receiving a 40 MHz clock and a 320 MHz clock from the test board.

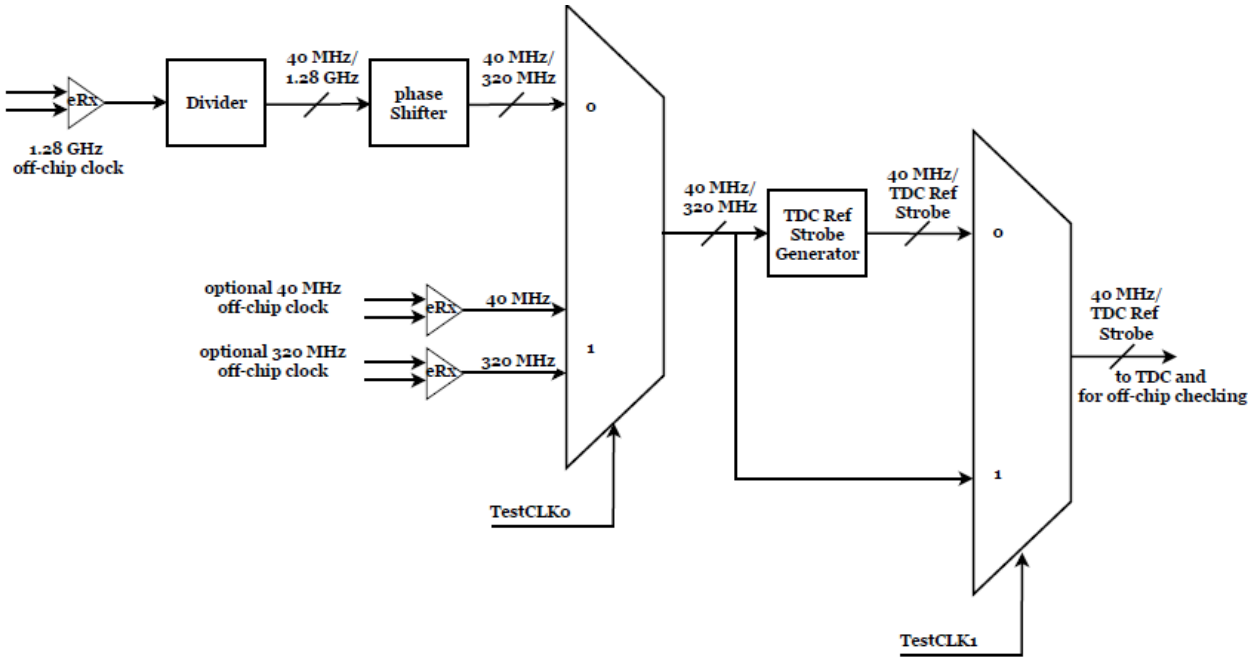

Figure 2.2.1 Block Diagram of the ETROC1 clock generator

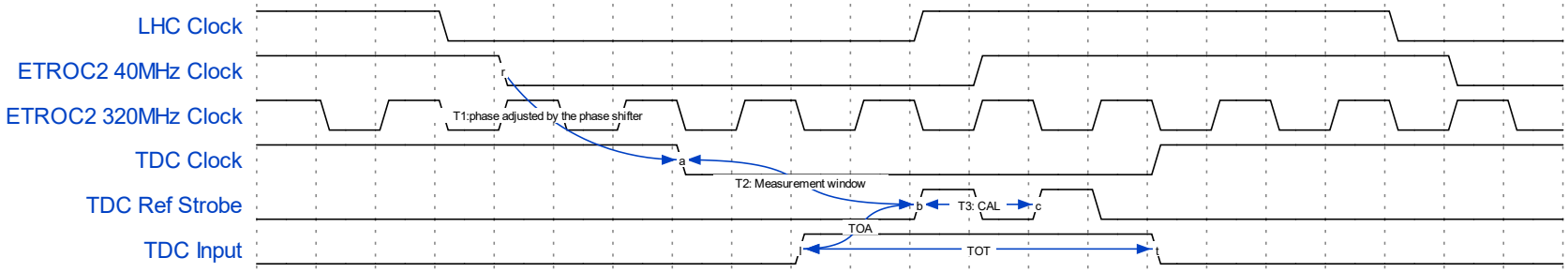

Figure 2.2.2 waveform of internal clock associated with TDC

2.3 PIXEL STRUCTURE

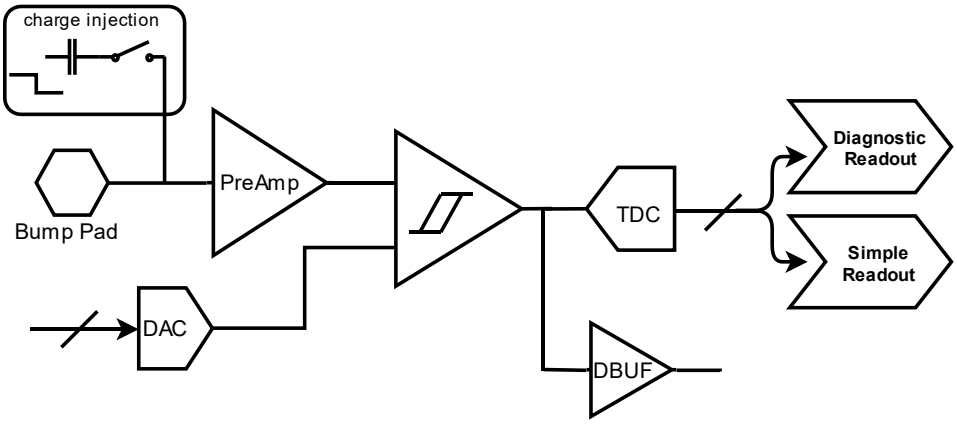

Figure 2.3.1 Pixel in array

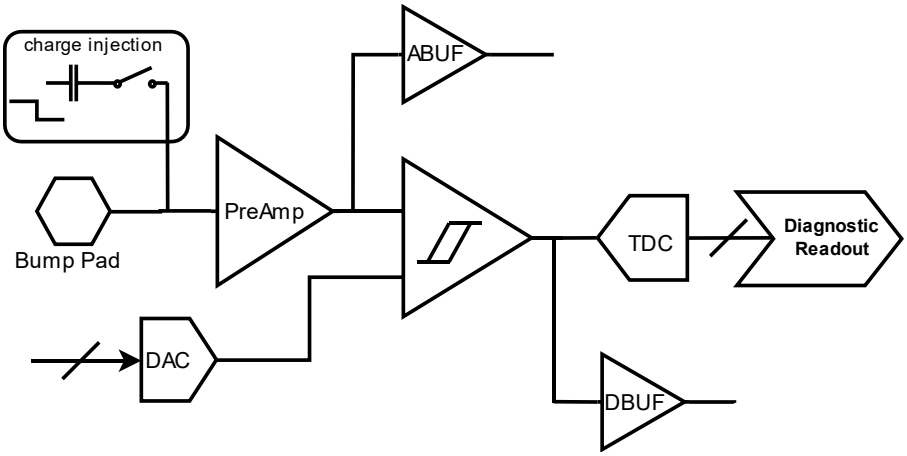

Figure 2.3.2 Standalone pixel

3 PINOUT

The suffixes, "_A", "_S" and "_T", represent the three blocks we have in ETROC1, array, standalone pixel and TDC, respectively. The opening of all the wire-bonding pads are 61 um by 126 um.

Table 1 Wire bonding pad of the standalone pixel

Num.	Name	Type	Description	Coordinate
1	RSTN_S	Digital input	I2C Reset	(4015.09, 8872.21)

2	SCL_S	Digital input	I2C clock	(3905.09, 8872.21)
3	SDA_S	Digital input	I2C data	(3795.09, 8872.21)
4	CLKTO_N_S	Differential output	Negative output of the test clock, either 40 MHz clock or 320 MHz pulse	(3685.09, 8872.21)
5	CLKTO_P_S		Positive output of the test clock, either 40 MHz clock or 320 MHz pulse	(3575.09, 8872.21)
6	vdd_Dig_S	Power	Power supply of the digital circuits, 1.2 V	(3465.09, 8872.21)
7	vss_Dig_S	Ground	Ground of the digital circuits, 0 V	(3355.09, 8872.21)
8	DOut_N_S	Differential output	1.28 Gbps data output of the standalone pixel, negative	(3245.09, 8872.21)
9	DOut_P_S		1.28 Gbps data output of the standalone pixel, positive	(3135.09, 8872.21)
10	QInj_N_S	Differential input	Negative input of the charge injection trigger	(3025.09, 8872.21)
11	QInj_P_S		Positive input of the charge injection trigger	(2915.09, 8872.21)
12	CLK40MI_N_S	Differential input	Negative input of the 40 MHz clock	(2805.09, 8872.21)
13	CLK40MI_P_S		Positive input of the 40 MHz clock	(2695.09, 8872.21)
14	CLK320MI_N_S	Differential input	Negative input of the 320 MHz clock	(2585.09, 8872.21)
15	CLK320MI_P_S		Positive input of the 320 MHz clock	(2475.09, 8872.21)
16	CLK1P28GI_N_S	Differential input	Negative input of the 1.28 GHz clock	(2365.09, 8872.21)

17	CLK1P28GI_P_S		Positive input of the 1.28 GHz clock	(2255.09, 8872.21)
18	vdd_Dig_S	Power	Power supply of the Tx and the Rx, 1.2 V	(2145.09, 8872.21)
19	vss_Dig_S	Ground	Ground of the Tx and the Rx, 0 V	(2035.09, 8872.21)
20	DiscriOut_S	Digital output	Discriminator output of the standalone pixel	(1925.09, 8872.21)
21	PAIn_S	Analog input	Input of the preamp	(1815.09, 8872.21)
22	PAIn_S	Analog input	Input of the preamp	(1705.09, 8872.21)
23	vdd_PA_S	Power	Power supply of the preamp, 1.2 V	(1595.09, 8872.21)
24	vss_PA_S	Ground	Ground of the preamp, 0 V	(1485.09, 8872.21)
25	VTHInOut_S	Analog output	DAC analog output	(1375.09, 8872.21)
26	VRef_S	Analog input	1 V reference input	(1265.09, 8872.21)
27	AOut_S	Analog output	Output of the analog buffer in the standalone pixel	(1155.09, 8872.21)
28	vdd_Buf_S	Power	Power supply of the analog buffer, 1.5 V	(1045.09, 8872.21)
29	vss_Buf_S	Ground	Ground of the analog buffer, 0	(935.09, 8872.21)
30	QV_S	Analog inout	Charge injection node Can be used to monitor voltage step size or to apply an external negative step	(825.09, 8872.21)
31	vdd_QInj_S	Power	Power supply of the charge injection, 1.2 V	(715.09, 8872.21)
32	vss_QInj_S	Ground	Ground of the charge injection, 0 V	(605.09, 8872.21)

33	vdd_Discri_S	Power	Power supply of the discriminator, 1.2 V	(495.09, 8872.21)
34	vss_Discri_S	Ground	Ground of the discriminator, 0 V	(385.09, 8872.21)

Table 2 Wire bonding pad of the array

Num.	Name	Type	Description	Coordinate
1	vdd_IO_A	Power	Power supply of the Tx and the Rx, 1.2 V	(1020,127.79)
2	vss_IO_A	Ground	Ground of the Tx and the Rx, 0 V	(1130,127.79)
3	CLK1P28GI_P_A	Differential input	Positive input of the 1.28 GHz clock	(1240,127.79)
4	CLK1P28GI_N_A		Negative input of the 1.28 GHz clock	(1350,127.79)
5	CLK320MI_P_A	Differential input	Positive input of the 320 MHz clock	(1460,127.79)
6	CLK320MI_N_A		Negative input of the 320 MHz clock	(1570,127.79)
7	CLK40MI_P_A	Differential input	Positive input of the 40 MHz clock	(1680,127.79)
8	CLK40MI_N_A		Negative input of the 40 MHz clock	(1790,127.79)
9	QInj_P_A	Differential input	Positive input of the charge injection trigger	(1900,127.79)
10	QInj_N_A		Negative input of the charge injection trigger	(2010,127.79)

11	CLKTO_P_A	Differential output	Positive output of the test clock, either 40 MHz clock or 320 MHz pulse	(2120,127.79)
12	CLKTO_N_A		Negative output of the test clock, either 40 MHz clock or 320 MHz pulse	(2230,127.79)
13	DOut_P_A	Differential output	Positive data output of the array, for either DMRO or SRO	(2340,127.79)
14	DOut_N_A		Negative data output of the array, for either DMRO or SRO	(2450,127.79)
15	vdd_IO_A	Power	Power supply of the Tx and the Rx, 1.2 V	(2560,127.79)
16	vss_IO_A	Ground	Ground of the Tx and the Rx, 0 V	(2670,127.79)
17	vdd_Discri_A	Power	Power supply of the discriminator, 1.2 V	(2780,127.79)
18	vss_Discri_A	Ground	Ground of the discriminator, 0 V	(2890,127.79)
19	vdd_PA _A	Power	Power supply of the preamp, 1.2 V	(3000,127.79)
20	vss_PA _A	Ground	Ground of the preamp, 0 V	(3110,127.79)
21	VRef _A	Analog input	1 V reference input	(3220,127.79)
22	vdd_PA _A	Power	Power supply of the preamp, 1.2 V	(3330,127.79)
23	vss_PA _A	Ground	Ground of the preamp, 0 V	(3440,127.79)
24	VTHInOut _A	Analog Inout	Threshold voltage of the discriminators	(3550,127.79)
25	vdd_PA	Power	Power supply of the preamp, 1.2 V	(3660,127.79)
26	vss_PA _A	Ground	Ground of the preamp, 0 V	(3770,127.79)
27	vdd_QInj _A	Power	Power supply of the charge injection, 1.2 V	(3880,127.79)

28	vss_QInj _A	Ground	Ground of the charge injection, 0 V	(3990,127.79)
29	vdd_CLK _A	Power	Power supply of the clocks generation circuits, 1.2 V	(4100,127.79)
30	vss_CLK _A	Ground	Ground of the clocks generation circuits, 0 V	(4210,127.79)
31	vdd_Discri _A	Power	Power supply of the discriminator, 1.2 V	(4320,127.79)
32	vss_Discri _A	Ground	Ground of the discriminator, 0 V	(4430,127.79)
33	vdd_Dig _A	Power	Power supply of the digital circuits, 1.2 V	(4540,127.79)
34	vss_Dig _A	Ground	Ground of the digital circuits, 0 V	(4650,127.79)
35	BC0_A	Digital input	Bunch crossing zero	(4760,127.79)
36	L1ACC _A	Digital input	Level-1 acceptance	(4870,127.79)
37	RSTN _A	Digital input	Reset for I2C/SRO Controller/DMRO internally pulled up	(4980,127.79)
38	DiscriOut _A	Digital output	Discriminator output of the array	(5090, 127.79)
39	A0_A	Digital input	I2C address low bit for the slave A	(5200,127.79)
40	A1_A	Digital input	I2C address high bit for the slave B	(5310,127.79)
41	vdd_Dig_A	Power	Power supply of the digital circuits, 1.2 V	(5420,127.79)
42	vss_Dig_A	Ground	Ground of the digital circuits, 0 V	(5530,127.79)
43	SCL_A_A	Digital input	I2C clock for the slave A	(5640,127.79)
44	SDA_ A_A	Digital input	I2C data for the slave A	(5750,127.79)

45	A0_B_A	Digital input	I2C address low bit for the slave A	(5860,127.79)
46	A1_B_A	Digital input	I2C address high bit for the slave B	(5970,127.79)
47	SCL_B_A	Digital input	I2C clock for the slave B	(6080,127.79)
48	SDA_ B_A	Digital input	I2C data for the slave B	(6190,127.79)
49	vdd_Dig_A	Power	Power supply of the digital circuits, 1.2 V	(6300,127.79)
50	vss_Dig_A	Ground	Ground of the digital circuits, 0 V	(6410,127.79)

Table 3 pinout of the TDC test block

Num.	Name	Type	Description	Coordinate
1	DOut_N_T	Digital Out	1.28G high speed serial data negative output	(6872.21, 8373.85)
2	DOut_P_T	Digital Out	1.28G high speed serial data positive output	(6872.21, 8450.03)
3	DMRO_vdd_T	Power supply	Power Supply of DMRO module, 1.2V	(6872.21, 8526.21)
4	DMRO_vss_T	Ground	Ground of the DMRO module	(6872.21, 8602.39)
5	CLK40MO_N_T	Digital Out	40M clock negative output	(6872.21, 8678.57)
6	CLK40MO_P_T	Digital Out	40M clock positive output	(6872.21, 8754.75)

7	I2C_vdd_T	Power Supply	Power supply of I2C module and Clock modules, 1.2V	(6720.68, 8872.21)
8	I2C_vss_T	Ground	Ground of I2C module and Clock modules	(6644.50, 8872.21)
9	CLK1P28GI_P_T	Digital In	1.28G clock positive input	(6563.92, 8872.21)
10	CLK1P28GI_N_T	Digital In	1.28G clock negative input	(6483.34, 8872.21)
11	CLK320MI_P _T	Digital In	320M clock positive input	(6402.76, 8872.21)
12	CLK320MI_N_T	Digital In	320M clock negative input	(6322.18, 8872.21)
13	CLK40MI_P_T	Digital In	40M clock positive input	(6241.61, 8872.21)
14	CLK40MI_N_T	Digital In	40M clock negative input	(6161.03, 8872.21)
15	Pulse_P_T	Analog In	Pulse positive input	(6080.45, 8872.21)
16	Pulse_N_T	Analog In	Pulse negative input	(5999.87, 8872.21)
17	TDC_vss_T	Ground	Ground of the TDC module	(5919.29, 8872.21)
18	TDC_vdd_T	Power supply	Power supply of the TDC module, 1.2V	(5843.11, 8872.21)
19	SCL_T	Digital In	I2C module serial clock	(5756.33, 8872.21)
20	SDA_T	Digital Out/In	I2C module serial data	(5651.26, 8872.21)
21	RSTN_T	Digital In	I2C module reset, low active	(5546.18, 8872.21)
22	A0_T	Digital In	I2C module external address select	(5441.11, 8872.21)

23	vss_GRO_T	Ground	Ground of Gate Ring Oscillator module.	(5350.91, 8872.21)
24	vdd_GRO_T	Power Suppl	Power supply of Gate Ring Oscillator module.	(5274.73 8872.21)
25	GRO_Out_P_T	Digital Out	Gate Ring Oscillator positive output	(5198.55, 8872.21)
26	GRO_Out_N_T	Digital Out	Gate Ring Oscillator negative output	(5122.37, 8872.21)

4 SLOW CONTROL

4.1 SLOW CONTROL FOR ARRAY

A generic I2C slave is used twice in ETROC1. Each slave provides 32 bytes for reading and 16 bytes for writing by ETROC1. A 4-bit chip ID and a 4-bit chip reversion are available as well. The registers in the I2C slave are triplicated to mitigate SEU. The registers in two slaves are named REG_A and REG_B, respectively. Their addresses are 7'b00000$A_{1_A}A_{0_A}$ and 7'b11111$A_{1_B}A_{0_B}$, respectively. Note that the address of 7'b0000000 should be avoided for the slave A.

Num.	REG. NAME	REG. ADDR.	Description	Default
1	CLSel[1:0]	REG_A_00[1:0]	Select of load capacitance of the preamp first stage 2`b00--> 0 fC 2`b01--> 80 fC 2`b10--> 80 fC 2`b01--> 160 fC Shared by all the pixels	2'b00
2	DIS_VTHInOut[15:0][a]	REG_A _03, REG_A _02	Disable threshold voltage input/output of the specified pixel. Active high. Each bit controls a pixel according the pixels index map. Only one of thresholds can be enabled at a time. For example, DIS_VTHInOut = 16'h4000	16'hffff

3	EN_DiscriOut[7:0]	REG_A _04	Enable the discriminator output. Active high. Each bit in EN_DiscriOut[7:4] represents the row, and each bit in EN_DiscriOut[3:0] represents the column. Users can enable the discriminator output from a specified pixel. Only one row can be specified at a time. **That means no more than one bit in EN_DiscriOut[7:4] can be set to 1'b1 at a time.** When more than one bit is set to 1'b1, or all bits are set to 0 in EN_DiscriOut[3:0], the discriminator output is disabled. For example: 8'b0010_0100→pixel in row 1 and column 2 8'b0001_0001→pixel in row 0 and column 0 8'b1000_0100→pixel in row 3 and column 2 8'bxxxx_0101→disable discriminator output, but invalid 8'b1011_ xxxx→invalid 8'b0000_0111→disable discriminator output 8'b0000_0000→disable discriminator output	8'b00010001
4	EN_QInj[15:0][a]	REG_A _06, REG_A _05	enable the charge injection of the specified pixel. Active high. Each bit controls a pixel. Users can specify non or more pixels to enable the charge injection.	16'h0001
5	HysSel[3:0]	REG_A _00[7:4]	Hysteresis voltage selection 4`b0000 --> Vhys1 4`b0001 --> Vhys2 4`b0011 --> Vhys3	4`b1111

			4`b0111 --> Vhys4 4`b1111 --> Vhys5 Vhys1 > Vhys2 > Vhys3 > Vhys4 = Vhys5 = 0 Shared by all the pixels	
6	IBSel[2:0]	REG_A _01[2:0]	Bias current selection of the input transistor in the preamp 3`b000 --> I1 3`b001, 3`b010, 3`b100 --> I2 3`b011, 3`b110, 3`b101 --> I3 3`b111 --> I4 I1 > I2 > I3 > I4 Shared by all the pixels	3`b111
7	OE_DMRO_Row[3:0]	REG_A _07[3:0]	Output enable of DMRO in rows. Each bit represents a row. Only one row can be enabled for output at a time. For example: 4'b0000→ no DMRO output enabled 4'b0001→ the row 0 of DMRO output is enabled 4'b0100→the row 2 of DMRO output is enable 4'b1010→invalid	4'b0001
8	DMRO_COL[1:0]	REG_A _07[5:4]	Select DMRO output from a specified column. 4'b00→column 0 4'b01→column 1 4'b10→column 2 4'b11→column 3	2'b00
9	RO_SEL	REG_A _07[6]	Select readout mode from either SRO or DMRO. 1'b0→DMRO enabled 1'b1→SRO enabled	1'b0
10	PD_DACDiscri[15:0]	REG_A _09, REG_A _08	Power down the DAC and the discriminator in pixels. Active high. Each bit controls a pixel. Users can specify non or more pixels to control.	16'h0000
11	QSel<4:0>	REG_A _01[7:3]	Select injected charge, from 1 fC(5`b00000) to 32 fC(5`b11111)	5'b00110

			Typical charge from LGAD sensor is 7 fC(5'b00110) Shared by all the pixels	
12	RfSel[1:0]	REG_A _00[3:2]	Feedback resistance selection 2`b00--> 20 kOHm 2`b01--> 10 kOHm 2`b10--> 5.7 kOHm 2`b11--> 4.4 kOHm Shared by all the pixels	2`b10
13	VTHIn[159:0]	REG_A _0A, REG_A _0B, REG_A _0C, REG_A _0D, REG_A _0E, REG_A _0F, REG_A _10, REG_A _11, REG_A _12, REG_A _13, REG_A _14, REG_A _15, REG_A _16, REG_A _17, REG_A _18, REG_A _19, REG_A _1A, REG_A _1B, REG_A _1C, REG_A _1D	Threshold voltage input of all the 16 pixels VTHIn[159:0]→{VTHIn15, VTHIn14, …, VTHIn1, VTHIn0} VTHIn15 represents DAC setting in pixel 15…	For each DAC, the default value is 10`b1000000000
14	autoReset_TDC	REG_B_00[0]		1'b0
15	enableMon_TDC	REG_B_00[1]	**This bit is actually used to control the readout test mode in ROTestGen.**	1'b0
16	enable_TDC	REG_B_00[2]		1'b1
17	level_TDC[2:0]	REG_B_01[2:0]		3'b001
18	offset_TDC[6:0]	REG_B_02[6:0]		7'b0000000
19	polaritySel_TDC	REG_B_00[3]		1'b1
20	resetn_TDC	REG_B_00[4]		1'b1
21	selRawCode_TDC	REG_B_00[5]		1'b0
22	testMode_TDC	REG_B_00[6]		1'b0
23	timeStampMode_TDC	REG_B_00[7]		1'b0
24	ROI[15:0]	REG_A_1F, REG_A_1E	Region of interest. 16-bit vector specifies which pixels are enabled for readout.	16'hffff

25	dllEnable	REG_B_03[0]	Enable loop control of DLL. The control voltage is tied to ground when dllEnable==low.	1'b1
26	dllForceDown	REG_B_03[1]	Force to pull down the output of the phase detector, active high.	1'b0
27	dllCapReset	REG_B_03[2]	Reset the control voltage of DLL to power supply, active high.	1'b0
28	dllCPCurrent[3:0]	REG_B_03[6:3]	Charge pump current control bits, ranging from 0 to 15uA for charge and discharge.	4'b0001
29	dllLate	REG_A_20[0]	Lock status prompt.	Read from ETROC1
30	PhaseAdj[7:0]	REG_B_04	Phase selecting control bits, PhaseAdj <7:3> for coarse, PhaseAdj <2:0> for fine.	8'b00000000
31	RefStrSel[7:0]	REG_B_05	TDC reference strobe selection.	8'b00000011,
32	ENScr_DMRO	REG_B_06[0]	Enable scrambling, active high	1'b1
33	REVCLK_DMRO	REG_B_06[1]	Reversing the clock used for input data latch, active-high. When REVData=0 data is latched at the rising edges of CLKWord, otherwise data is latched at the falling edges of CLKWord.	1'b0
34	REVData_DMRO	REG_B_06[2]	reversing input data, active-high.	1'b0
35	TestMode_DMRO	REG_B_06[3]	Test mode input, active high. The PRBS7 is sent out in test mode (TestMode == 1) while the data is sent out in normal mode (TestMode == 0).	1'b0
36	TestCLK0	REG_B_06[4]	When TestCLK0=1, the phase shifter is bypassed and off-chip 40MHz and 320MHz are used.	1'b0
37	TestCLK1	REG_B_06[5]	When TestCLK1=1, the TDC reference strobe generator is bypassed and off-chip 40MHz and 320MHz are used.	1'b0
38	CLKOutSel	REG_B_06[6]	Select output from either 40 MHz clock or TDC reference strobe 1'b0: 40 MHz clock 1'b1: TDC reference strobe	1'b1

39	enableRx_1P28G	REG_B_07[5]	Enable the Rx for 1.28 GHz clock, active high	1'b1
40	setCM_1P28G	REG_B_07[4]	Set common voltage of the Rx for the 1.28 GHz clock to ½ vdd, active high	1'b1
41	enableTER_1P28G	REG_B_07[3]	Enable internal termination of the Rx for the 1.28 GHz clock, active high	1'b1
42	invertData_1P28G	REG_B_07[2]	Invert data of the Rx for the 1.28 GHz clock, active high	1'b0
43	equ_1P28G[1:0]	REG_B_07[1:0]	Equalization strength of the Rx for the 320 MHz clock 2'b00, equalization is turned off 2'b11, largest equalization	2'b00
44	enableRx_320M	REG_B_08[5]	Enable the Rx for the 320 MHz clock, active high	1'b0
45	setCM_320M	REG_B_08[4]	Set common voltage of the Rx for the 320 MHz clock to ½ vdd, active high	1'b1
46	enableTER_320M	REG_B_08[3]	Enable internal termination of the Rx for the 320 MHz clock, active high	1'b1
47	invertData_320M	REG_B_08[2]	Invert data of the Rx for the 320 MHz clock, active high	1'b0
48	equ_320M [1:0]	REG_B_08[1:0]	Equalization strength of the Rx for the 320 MHz clock 2'b00, equalization is turned off 2'b11, largest equalization	2'b00
49	enableRx_40M	REG_B_09[5]	Enable the Rx for the 40 MHz clock, active high	1'b0
50	setCM_40M	REG_B_09[4]	Set common voltage of the Rx for the 40 MHz clock to ½ vdd, active high	1'b1
51	enableTER_40M	REG_B_09[3]	Enable internal termination of the Rx for the 40 MHz clock, active high	1'b1
52	invertData_40M	REG_B_09[2]	Invert data of the Rx for the 40 MHz clock, active high	1'b0
53	equ_40M [1:0]	REG_B_09[1:0]	Equalization strength of the Rx for the 40 MHz clock 2'b00, equalization is turned off 2'b11, largest equalization	2'b00
54	enableRx_QInj	REG_B_0A[5]	Enable the Rx for the QInj, active high	1'b1

55	setCM_QInj	REG_B_0A[4]	Set common voltage of the Rx for the QInj to ½ vdd, active high	1'b1
56	enableTER_QInj	REG_B_0A[3]	Enable internal termination of the Rx for the QInj, active high	1'b1
57	invertData_QInj	REG_B_0A[2]	Invert data of the Rx for the QInj, active high	1'b0
58	equ_QInj [1:0]	REG_B_0A[1:0]	Equalization strength of the Rx for the QInj 2'b00, equalization is turned off 2'b11, largest equalization	2'b00
59	AMPL_CLKTO[2:0]	REG_B_0B[2:0]	3bits to select different output amplitude. 3b'000 = min amplitude(50m) 3b'111 = max amplitude(320m) Step size ≈ 40mV	3'b111
60	disCML_CLKTO	REG_B_0B[3]	Disable CML driver, active high	1'b0
61	AMPL_DOut[2:0]	REG_B_0B[6:4]	3bits to select different output amplitude. 3b'000 = min amplitude(50m) 3b'111 = max amplitude(320m) Step size ≈ 40mV	3'b111
	disCML_DOut	REG_B_0B[7]	Disable CML driver, active high	1'b0
62				
63				

a. See the pixel index map below

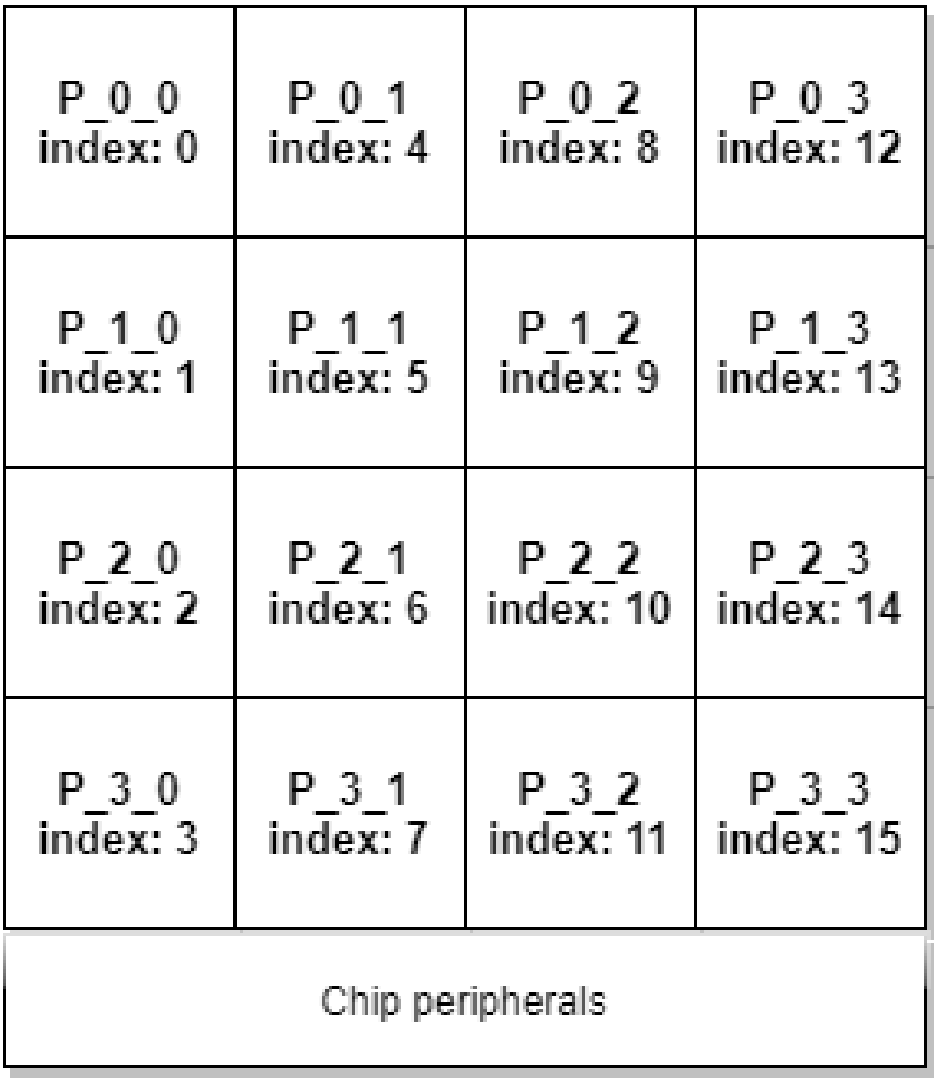

Figure 4.1 Pixels index map

ADDR. (Hex)	BIT								Default (Hex)
	7	6	5	4	3	2	1	0	
REG_A_00	HysSel[3]	HysSel[2]	HysSel[1]	HysSel[0]	RfSel[1]	RfSel[0]	CLSel[1]	CLSel[0]	F8
REG_A_01	QSel[4]	QSel[3]	QSel[2]	QSel[1]	QSel[0]	IBSel[2]	IBSel[1]	IBSel[0]	37
REG_A_02	DIS_VTHInOut[7]	DIS_VTHInOut [6]	DIS_VTHInOut [5]	DIS_VTHInOut [4]	DIS_VTHInOut [3]	DIS_VTHInOut [2]	DIS_VTHInOut [1]	DIS_VTHInOut [0]	FF
REG_A_03	DIS_VTHInOut[15]	DIS_VTHInOut[14]p	DIS_VTHInOut[13]	DIS_VTHInOut[12]	DIS_VTHInOut [11]	DIS_VTHInOut [10]	DIS_VTHInOut [9]	DIS_VTHInOut [8]	FF
REG_A_04	EN_DiscriOut[7]	EN_DiscriOut[6]	EN_DiscriOut[5]	EN_DiscriOut[4]	EN_DiscriOut[3]	EN_DiscriOut[2]	EN_DiscriOut[1]	EN_DiscriOut[0]	11
REG_A_05	EN_QInj[7]	EN_QInj [6]	EN_QInj[5]	EN_QInj[4]	EN_QInj [3]	EN_QInj [2]	EN_QInj [1]	EN_QInj [0]	01
REG_A_06	EN_QInj[15]	EN_QInj[14]	EN_QInj[13]	EN_QInj[12]	EN_QInj[11]	EN_QInj[10]	EN_QInj [9]	EN_QInj [8]	00
REG_A_07	X	RO_SEL	DMRO_COL[1]	DMRO_COL[0]	OE_DMRO_Row[3]	OE_DMRO_Row[2]	OE_DMRO_Row[1]	OE_DMRO_Row[0]	01
REG_A_08	PD_DACDiscri[7]	PD_DACDiscri [6]	PD_DACDiscri [5]	PD_DACDiscri [4]	PD_DACDiscri [3]	PD_DACDiscri [2]	PD_DACDiscri [1]	PD_DACDiscri [0]	00
REG_A_09	PD_DACDiscri[15]	PD_DACDiscri[14]	PD_DACDiscri[13]	PD_DACDiscri[12]	PD_DACDiscri [11]	PD_DACDiscri [10]	PD_DACDiscri [9]	PD_DACDiscri [8]	00
REG_A_0A	VTHIn[7]	VTHIn[6]	VTHIn[5]	VTHIn[4]	VTHIn[3]	VTHIn[2]	VTHIn[1]	VTHIn[0]	00
REG_A_0B	VTHIn[15]	VTHIn[14]	VTHIn[13]	VTHIn[12]	VTHIn[11]	VTHIn[10]	VTHIn[9]	VTHIn[8]	02
REG_A_0C	VTHIn[23]	VTHIn[22]	VTHIn[21]	VTHIn[20]	VTHIn[19]	VTHIn[18]	VTHIn[17]	VTHIn[16]	08
REG_A_0D	VTHIn[31]	VTHIn[30]	VTHIn[29]	VTHIn[28]	VTHIn[27]	VTHIn[26]	VTHIn[25]	VTHIn[24]	20
REG_A_0E	VTHIn[39]	VTHIn[38]	VTHIn[37]	VTHIn[36]	VTHIn[35]	VTHIn[34]	VTHIn[33]	VTHIn[32]	80
REG_A_0F	VTHIn[47]	VTHIn[46]	VTHIn[45]	VTHIn[44]	VTHIn[43]	VTHIn[42]	VTHIn[41]	VTHIn[40]	00
REG_A_10	VTHIn[55]	VTHIn[54]	VTHIn[53]	VTHIn[52]	VTHIn[51]	VTHIn[50]	VTHIn[49]	VTHIn[48]	02
REG_A_11	VTHIn[63]	VTHIn[62]	VTHIn[61]	VTHIn[60]	VTHIn[59]	VTHIn[58]	VTHIn[57]	VTHIn[56]	08
REG_A_12	VTHIn[71]	VTHIn[70]	VTHIn[69]	VTHIn[68]	VTHIn[67]	VTHIn[66]	VTHIn[65]	VTHIn[64]	20
REG_A_13	VTHIn[79]	VTHIn[78]	VTHIn[77]	VTHIn[76]	VTHIn[75]	VTHIn[74]	VTHIn[73]	VTHIn[72]	80
REG_A_14	VTHIn[87]	VTHIn[86]	VTHIn[85]	VTHIn[84]	VTHIn[83]	VTHIn[82]	VTHIn[81]	VTHIn[80]	00
REG_A_15	VTHIn[95]	VTHIn[94]	VTHIn[93]	VTHIn[92]	VTHIn[91]	VTHIn[90]	VTHIn[89]	VTHIn[88]	02
REG_A_16	VTHIn[103]	VTHIn[102]	VTHIn[101]	VTHIn[100]	VTHIn[99]	VTHIn[98]	VTHIn[97]	VTHIn[96]	08
REG_A_17	VTHIn[111]	VTHIn[110]	VTHIn[109]	VTHIn[108]	VTHIn[107]	VTHIn[106]	VTHIn[105]	VTHIn[104]	20
REG_A_18	VTHIn[119]	VTHIn[118]	VTHIn[117]	VTHIn[116]	VTHIn[115]	VTHIn[114]	VTHIn[113]	VTHIn[112]	80
REG_A_19	VTHIn[127]	VTHIn[126]	VTHIn[125]	VTHIn[124]	VTHIn[123]	VTHIn[122]	VTHIn[121]	VTHIn[120]	00
REG_A_1A	VTHIn[135]	VTHIn[134]	VTHIn[133]	VTHIn[132]	VTHIn[131]	VTHIn[130]	VTHIn[129]	VTHIn[128]	02
REG_A_1B	VTHIn[143]	VTHIn[142]	VTHIn[141]	VTHIn[140]	VTHIn[139]	VTHIn[138]	VTHIn[137]	VTHIn[136]	08
REG_A_1C	VTHIn[151]	VTHIn[150]	VTHIn[149]	VTHIn[148]	VTHIn[147]	VTHIn[146]	VTHIn[145]	VTHIn[144]	20

REG_A_1D	VTHIn[159]	VTHIn[158]	VTHIn[157]	VTHIn[156]	VTHIn[155]	VTHIn[154]	VTHIn[153]	VTHIn[152]	80
REG_A_1E	ROI[7]	ROI[6]	ROI[5]	ROI[4]	ROI[3]	ROI[2]	ROI[1]	ROI[0]	FF
REG_A_1F	ROI[15]	ROI[14]	ROI[13]	ROI[12]	ROI[11]	ROI[10]	ROI[9]	ROI[8]	FF
REG_B_00	timeStampMode_TDC	testMode_TDC	selRawCode_TDC	resetn_TDC	polaritySel_TDC	enable_TDC	enableMon_TDC	autoReset_TDC	1C
REG_B_01	X	X	X	X	X	level_TDC[2]	level_TDC[1]	level_TDC[0]	01
REG_B_02	X	offset_TDC[6]	offset_TDC[5]	offset_TDC[4]	offset_TDC[3]	offset_TDC[2]	offset_TDC[1]	offset_TDC[0]	00
REG_B_03	X	dllCPCurrent[3]	dllCPCurrent[2]	dllCPCurrent[1]	dllCPCurrent[0]	dllCapReset	dllForceDown	dllEnable	09
REG_B_04	PhaseAdj[7]	PhaseAdj[6]	PhaseAdj[5]	PhaseAdj[4]	PhaseAdj[3]	PhaseAdj[2]	PhaseAdj[1]	PhaseAdj[0]	00
REG_B_05	RefStrSel[7]	RefStrSel[6]	RefStrSel[5]	RefStrSel[4]	RefStrSel[3]	RefStrSel[2]	RefStrSel[1]	RefStrSel[0]	03
REG_B_06	X	CLKOutSel	TestCLK1	TestCLK0	TestMode_DMRO	REVData_DMRO	REVCLK_DMRO	ENScr_DMRO	41
REG_B_07	X	X	enableRx_1P28G	setCM_1P28G	enableTER_1P28G	invertData_1P28G	equ_1P28G[1]	equ_1P28G[0]	38
REG_B_08	X	X	enableRx_320M	setCM_320M	enableTER_320M	invertData_320M	equ_320M[1]	equ_320M[0]	18
REG_B_09	X	X	enableRx_40M	setCM_40M	enableTER_40M	invertData_40M	equ_40M[1]	equ_40M[0]	18
REG_B_0A	X	X	enableRx_QInj	setCM_QInj	enableTER_QInj	invertData_QInj	equ_ QInj[1]	equ_ QInj[0]	38
REG_B_0B	disCML_DOut	AMPL_DOut[2]	AMPL_DOut[1]	AMPL_DOut[0]	disCML_CLKTO	AMPL_CLKTO[2]	AMPL_CLKTO[1]	AMPL_CLKTO[0]	77

4.2 SLOW CONTROL FOR FULL PIXEL

A generic I2C slave is used in ETROC1 Full Pixel Test Block. The slave provides 32 bytes for reading and 16 bytes for writing by ETROC1. A 4-bit chip ID and a 4-bit chip reversion are available as well. The registers in the I2C slave are triplicated to mitigate SEU. The Slave addresses is 7'b1001110.

Num.	REG. NAME	REG. ADDR.	Description	Default
1	autoReset_TDC	REG_00[0]	TDC autoReset mode	1'b0
2	enableMon_TDC	REG_00[1]	~~Enable TDC Raw data output~~ Control of readout test mode in ROTestGen.	1'b0
3	enable_TDC	REG_00[2]	Enable TDC	1'b1
4	polaritySel_TDC	REG_00[3]	TDC Controller control signal polarity select	1'b1
5	resetn_TDC	REG_00[4]	Reset TDC, low active	1'b1
6	selRawCode_TDC	REG_00[5]	Select Row data or combination data	1'b0

7	testMode_TDC	REG_00[6]	TDC test mode select	1'b0
8	timeStampMode_TDC	REG_00[7]	Calibration data timestamp mode	1'b0
9	level_TDC[2:0]	REG_01[2:0]	Bubble level	3'b001
10	offset_TDC[6:0]	REG_02[6:0]	Ripple counter window offest	7'b0000000
11	dllEnable	REG_03[0]	Enable loop control of DLL. The control voltage is tied to ground when dllEnable==low.	1'b1
12	dllForceDown	REG_03[1]	Force to pull down the output of the phase detector, active high.	1'b0
13	dllCapReset	REG_03[2]	Reset the control voltage of DLL to power supply, active high.	1'b0
14	dllCPCurrent[3:0]	REG_03[6:3]	Charge pump current control bits, ranging from 0 to 15uA for charge and discharge.	4'b0001
15	dllLate	REG_20[0]	Lock status prompt.	Read from ETROC1
16	PhaseAdj[7:0]	REG_04	Phase selecting control bits, PhaseAdj <7:3> for coarse, PhaseAdj <2:0> for fine.	8'b00000000
17	RefStrSel[7:0]	REG_05	TDC reference strobe selection.	8'b00000011,
18	RSTN_DMRO	REG_06[0]	DMRO Reset, active low	1'b1
19	ENScr_DMRO	REG_06[1]	Enable scrambling, active high	1'b1
20	REVCLK_DMRO	REG_06[2]	Reversing the clock used for input data latch, active-high. When REVData=0 data is latched at the rising edges of CLKWord, otherwise data is latched at the falling edges of CLKWord.	1'b0
21	REVData_DMRO	REG_06[3]	reversing input data, active-high.	1'b0
22	TestMode_DMRO	REG_06[4]	Test mode input, active high. The PRBS7 is sent out in test mode (TestMode == 1) while the data is sent out in normal mode (TestMode == 1).	1'b0
23	TestCLK0	REG_06[5]	When TestCLK0=1, the phase shifter is bypassed and off-chip 40MHz and 320MHz are used.	1'b0
24	TestCLK1	REG_06[6]	When TestCLK1=1, the TDC reference strobe generator is bypassed and off-chip 40MHz and 320MHz are used.	1'b0

25	CLKOutSel	REG_06[7]	Select output from either 40 MHz clock or TDC reference strobe 1'b0: 40 MHz clock 1'b1: TDC reference strobe	1'b1
26	enableRx_1P28G	REG_07[5]	Enable the Rx for 1.28 GHz clock, active high	1'b1
27	setCM_1P28G	REG_07[4]	Set common voltage of the Rx for the 1.28 GHz clock to ½ vdd, active high	1'b1
28	enableTER_1P28G	REG_07[3]	Enable internal termination of the Rx for the 1.28 GHz clock, active high	1'b1
29	invertData_1P28G	REG_07[2]	Invert data of the Rx for the 1.28 GHz clock, active high	1'b0
30	equ_1P28G[1:0]	REG_07[1:0]	Equalization strength of the Rx for the 320 MHz clock 2'b00, equalization is turned off 2'b11, largest equalization	2'b00
31	enableRx_320M	REG_08[5]	Enable the Rx for the 320 MHz clock, active high	1'b0
32	setCM_320M	REG_08[4]	Set common voltage of the Rx for the 320 MHz clock to ½ vdd, active high	1'b1
33	enableTER_320M	REG_08[3]	Enable internal termination of the Rx for the 320 MHz clock, active high	1'b1
34	invertData_320M	REG_08[2]	Invert data of the Rx for the 320 MHz clock, active high	1'b0
35	equ_320M [1:0]	REG_08[1:0]	Equalization strength of the Rx for the 320 MHz clock 2'b00, equalization is turned off 2'b11, largest equalization	2'b00
36	enableRx_40M	REG_09[5]	Enable the Rx for the 40 MHz clock, active high	1'b0
37	setCM_40M	REG_09[4]	Set common voltage of the Rx for the 40 MHz clock to ½ vdd, active high	1'b1
38	enableTER_40M	REG_09[3]	Enable internal termination of the Rx for the 40 MHz clock, active high	1'b1
39	invertData_40M	REG_09[2]	Invert data of the Rx for the 40 MHz clock, active high	1'b0
40	equ_40M [1:0]	REG_09[1:0]	Equalization strength of the Rx for the 40 MHz clock	2'b00

			2’b00, equalization is turned off 2’b11, largest equalization	
41	enableRx_QInj	REG_0A[5]	Enable the Rx for the QInj, active high	1’b1
42	setCM_QInj	REG_0A[4]	Set common voltage of the Rx for the QInj to ½ vdd, active high	1’b1
43	enableTER_QInj	REG_0A[3]	Enable internal termination of the Rx for the QInj, active high	1’b1
44	invertData_QInj	REG_0A[2]	Invert data of the Rx for the QInj, active high	1’b0
45	equ_QInj [1:0]	REG_0A[1:0]	Equalization strength of the Rx for the QInj 2’b00, equalization is turned off 2’b11, largest equalization	2’b00
46	AMPL_ CLKTO[2:0]	REG_0B[2:0]	3bits to select different output amplitude. 3b’000 = min amplitude(50m) 3b’111 = max amplitude(320m) Step size ≈ 40mV	3’b111
47	disCML_CLKTO	REG_0B[3]	Disable CML driver, active high	1’b0
48	AMPL_DOut[2:0]	REG_0B[6:4]	3bits to select different output amplitude. 3b’000 = min amplitude(50m) 3b’111 = max amplitude(320m) Step size ≈ 40mV	3’b111
49	disCML_DOut	REG_0B[7]	Disable CML driver, active high	1’b0
50	CLSel[1:0]	REG_0C[1:0]	Select of load capacitance of the preamp first stage 2`b00--> 0 fC 2`b01--> 80 fC 2`b10--> 80 fC 2`b01--> 160 fC Shared by all the pixels	2’b00
51	RfSel[1:0]	REG_0C[3:2]	Feedback resistance selection 2`b00--> 20 kOHm 2`b01--> 10 kOHm 2`b10--> 5.7 kOHm 2`b11--> 4.4 kOHm Shared by all the pixels	2`b10
52	HysSel[3:0]	REG_0C[7:4]	Hysteresis voltage selection 4`b0000 --> Vhys1 4`b0001 --> Vhys2 4`b0011 --> Vhys3 4`b0111 --> Vhys4	4`b1111

			4`b1111 --> Vhys5 Vhys1 > Vhys2 > Vhys3 > Vhys4 = Vhys5 = 0 Shared by all the pixels	
53	IBSel[2:0]	REG_0D[2:0]	Bias current selection of the input transistor in the preamp 3`b000 --> I1 3`b001, 3`b010, 3`b100 --> I2 3`b011, 3`b110, 3`b101 --> I3 3`b111 --> I4 I1 > I2 > I3 > I4 Shared by all the pixels	3`b111
54	QSel[4:0]	REG_0D[7:3]	Select injected charge, from 1 fC(5`b00000) to 32 fC(5`b11111) Typical charge from LGAD sensor is 7 fC(7`b0000110) Shared by all the pixels	5'b00110
55	VTHIn[9:0]	REG_0E[7:0] REG_0F[1:0]	Threshold voltage input of Discriminator , VTHIn[9:0] represents DAC setting REG_0F[1:0] go to VTHIn[9:8]	10`b1000000000
56	EN_QInj	REG_0F[2]	enable the charge injection	1'b1
57	EN_DiscriOut	REG_0F[3]	Enable Discriminator Output	1'b0
58	Dis_VTHInOut	REG_0F[4]	Disable VTHIn Output	1'b1
59	PD_DACDiscri	REG_0F[5]	Power down the DAC and the discriminator, active low	1'b0
60	OE_DMRO	REG_0F[6]	Output enable of DMRO	1'b1

4.3 SLOW CONTROL FOR TDC TEST BLOCK

A generic I2C slave is used in ETROC1 TDC Test Block. The slave provides 32 bytes for writing and 16 bytes for reading by ETROC1. A 4-bit chip ID and a 4-bit chip reversion are available as well. The registers in the I2C slave are triplicated to mitigate SEU. The Slave addresses is 7'b010001X, The LSB of address is determined by pad A0.

1	Dataout_disCMLDriver_BIAS	REG_00[0]	Disable Dataout CML Driver	1'b0
2	Clk40Mout_disCMLDriver_BIAS	REG_00[1]	Disable Clk40M CML Driver	1'b0
3	tdc_offset<6:0>	REG_01[6:0]	TDC ripple counter metastability window offset.	7'b0000000

4	tdc_enable	REG_01[7]	TDC enable	1'b1
5	tdc_level<2:0>	REG_02[2:0]	TDC Encoder bubble tolerance.	3'b001
6	tdc_testMode	REG_02[3]	TDC Test Mode	1'b0
7	tdc_selRawCode	REG_02[4]	Select TDC Raw code, always "0"	1'b0
8	tdc_resetn	REG_02[5]	TDC reset signal	1'b1
9	tdc_polaritySel	REG_02[6]	TDC controller output signal polarity	1'b1
10	tdc_autoReset	REG_02[7]	TDC automatic reset signal	1'b0
11	Clk40Mout_AmplSel<2:0>	REG_03[2:0]	40 MHz clock CML output Amplitude select	3'b001
12	tdc_enableMon	REG_03[3]	Enable TDC raw data output	1'b1
13	tdc_timeStampMode	REG_03[4]	TDC Calibration data timeStamp Mode	1'b0
14	Dataout_AmplSel<2:0>	REG_04[2:0]	1.28 GHz Serial data output Amplitude select	3'b001
15	ro_testmode	REG_04[3]	DMRO test mode select	1'b0
16	ro_enable	REG_04[4]	Enable DMRO	1'b1
17	ro_reverse	REG_04[5]	DMRO output data reverse	1'b0
18	ro_resetn	REG_04[6]	DMRO reset, low active	1'b1
19	ro_revclk	REG_04[7]	DMRO 40 MHz clock reverse	1'b0
20	Dataout_Sel	REG_05[0]	1.28GHz data output when asserted, 320MHz clock pulse output when deserted	1'b1
21	Clk320M_Psel	REG_05[1]	320M Pulse clock comes from external when asserted, otherwise comes from internal	1'b1
22	Clk40M_Psel	REG_05[2]	40M Pulse clock comes from external when asserted, otherwise comes from internal	1'b1
23	Clk320M_Sel	REG_05[3]	320M clock comes from internal divider when asserted, otherwise	1'b1

			comes from external input.	
24	Clk40M_Sel	REG_05[4]	40M clock comes from internal divider when asserted, otherwise comes from external input.	1'b1
25	Pulse_Sel<7:0>	REG_06[7:0]	320M clock pulse location select	8'b00000011
26	Clk40M_equalizer<1:0>	REG_07[1:0]	40M clock input eRx equalizer intensity	2'b00
27	Clk40M_invertData	REG_07[2]	40M clock input eRx data invert	1'b0
28	Clk40M_enableTermination	REG_07[3]	Enable 40M clock input eRx termination	1'b1
29	Clk40M_setCommonMode	REG_07[4]	Set 40M clock input eRx common mode	1'b1
30	Clk40M_enableRx	REG_07[5]	Enable 40M clock input eRx	1'b1
31	Clk320M_equalizer<1:0>	REG_08[1:0]	320M clock input eRx equalizer intensity	2'b00
32	Clk320M_invertData	REG_08[2]	320M clock input eRx data invert	1'b0
33	Clk320M_enableTermination	REG_08[3]	Enable 320M clock input eRx termination	1'b1
34	Clk320M_setCommonMode	REG_08[4]	Set 320M clock input eRx common mode	1'b1
35	Clk320M_enableRx	REG_08[5]	Enable 320M clock input eRx	1'b1
36	Clk1G28_equalizer<1:0>	REG_09[1:0]	1.28G clock input eRx equalizer intensity	2'b00
37	Clk 1G28_invertData	REG_09[2]	1.28G clock input eRx data invert	1'b0
38	Clk1G28_enableTermination	REG_09[3]	Enable 1.28G clock input eRx termination	1'b1
39	Clk1G28_setCommonMode	REG_09[4]	Set 1.28G clock input eRx common mode	1'b1
40	Clk 1G28_enableRx	REG_09[5]	Enable 1.28G clock input eRx	1'b1
41	Pulse_equalizer<1:0>	REG_0A[1:0]	TDC pulse input eRx equalizer intensity	2'b00

42	Pulse_invertData	REG_0A[2]	TDC pulse input eRx data invert	1'b0
43	Pulse_enableTermination	REG_0A[3]	Enable TDC pulse input eRx termination	1'b1
44	Pulse_setCommonMode	REG_0A[4]	Set pulse input eRx common mode	1'b1
45	Pulse_enableRx	REG_0A[5]	Enable pulse input eRx	1'b1
46	TDCRawData_Sel	REG_0B[0]	TDC Raw data group select	1'b1
47	GRO_TOT_CK	REG_0B[1]	GRO TOT clock	1'b1
48	GRO_TOTRST_N	REG_0B[2]	GRO TOT Reset, active low	1'b1
49	GRO_TOA_Latch	REG_0B[3]	GRO TOA Latch clock	1'b1
50	GRO_TOA_CK	REG_0B[4]	GRO TOA clock	1'b1
51	GRO_TOARST_N	REG_0B[5]	GRO TOA Reset, low active	1'b1
52	GRO_Start	REG_0B[6]	GRO Start signal, high active	1'b0
53	GROout_disCMLDriver_BIASA/B/C	REG_0C[0]	Disable GRO output CML Driver	1'b0
54	GROout_AmplSel<2:0>	REG_0C[3:1]	GRO output CML Driver Amplitude selection	3'b001

TDC Test block read-only register:

		TDCRawData_Sel = 0	**TDCRawData_Sel = 1**
1	REG_20[2:0]	CalCounterBMon<2:0>	TOACounterBMon<2:0>
2	REG_20[5:3]	CalCounterAMon<2:0>	TOACounterAMon<2:0>
3	REG_20[6]	CalerrorFlagReg	TOAerrorFalgReg
4	REG_21[7:0]	TOT_codeReg<7:0>	TOARawDataMon<7:0>
5	REG_22[7:0]	TOA_codeReg<6:0>, TOT_codeReg<8>	TOARawDataMon<15:8>
6	REG_23[7:0]	Cal_codeReg<4:0>, TOA_codeReg<9:7>	TOARawDataMon<23:16>
7	REG_24[7:0]	CalRawDataMon<31:29>,Cal_codeReg<9:5>	TOARawDataMon<31:24>
8	REG_25[7:0]	CalRawDataMon<39:32>	TOARawDataMon<39:32>
9	REG_26[7:0]	CalRawDataMon<47:40>	TOARawDataMon<47:40>
10	REG_27[7:0]	CalRawDataMon<55:48>	TOARawDataMon<55:48>
11	REG_28[6:0]	CalRawDataMon<62:56>	TOARawDataMon<62:56>
12	REG_29[7:0]	HitFalg, TOTerrorFlagReg, TOTCounterAMon<2:0>, TOTCounterBMon<2:0>	
13	REG_2A[7:0]	CalRawDataMon<7:0>	TOTRawDataMon<7:0>

14	REG_2B[7:0]	CalRawDataMon<15:8>	TOTRawDataMon<15:8>
15	REG_2C[7:0]	CalRawDataMon<23:16>	TOTRawDataMon<23:16>
16	REG_2D[7:0]	<*3>Low,CalRawDataMon<28:24>	TOTRawDataMon<31:24>
17	REG_2E[5:0]	DBF_QC<5:0>	RO_DBF_QC<5:0>

5 BUILDING BLOCKS DESIGN

5.1 PREAMP

The preamplifier consists of a two-stage amplifier. A cascode amplifier with resistive feedback acts as the first stage, and a source follower as the second stage. The size of each transistor in the preamplifier has been optimized by using an LGAD simulation as the input signal. The design considers both leading and trailing edge to optimize the TOT measurement for the time-walk correction. The feedback resistance is programmable to allow adjustment of the fall time, while the bias current is also programmable to allow different trade-offs between power consumption and performance. The load capacitance of the first stage is also programmable to allow optimization of the bandwidth.

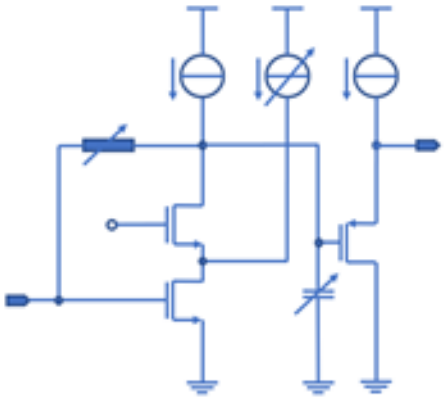

Figure 5.1 Block diagram of Preamplifier

5.2 DISCRIMINATOR

The discriminator, with a user programmable threshold controlled by an internal DAC, is optimized for the full chain for low signal size while keeping power consumption low.

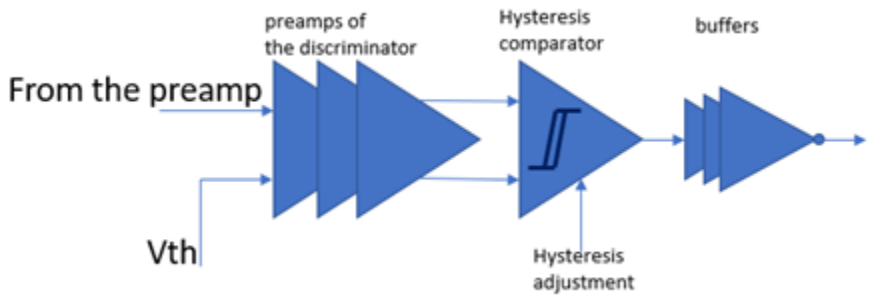

Figure 5.2 Block diagram of Discriminator

5.3 TDC

5.3.1 TDC Core

5.3.2 Phase shifter

The phase shifter circuit aims at producing a programmable phase rotation (up to 360 degree) with a time resolution of 97.6 ps for 320 MHz and 40 MHz clock frequencies. The circuit is implemented as two functional blocks: a coarse phase shifter, with a fully digital implementation, and fine phase shifter, based on a Delay-Line Loop (DLL).

The coarse phase-shifter block is responsible for selecting the appropriate clock frequency and to set the clock phase with a resolution of 781.25 ps (period of 1.28 GHz), while the fine phase shifter further interpolates within the 781.25 ps interval down to 97.6 ps.

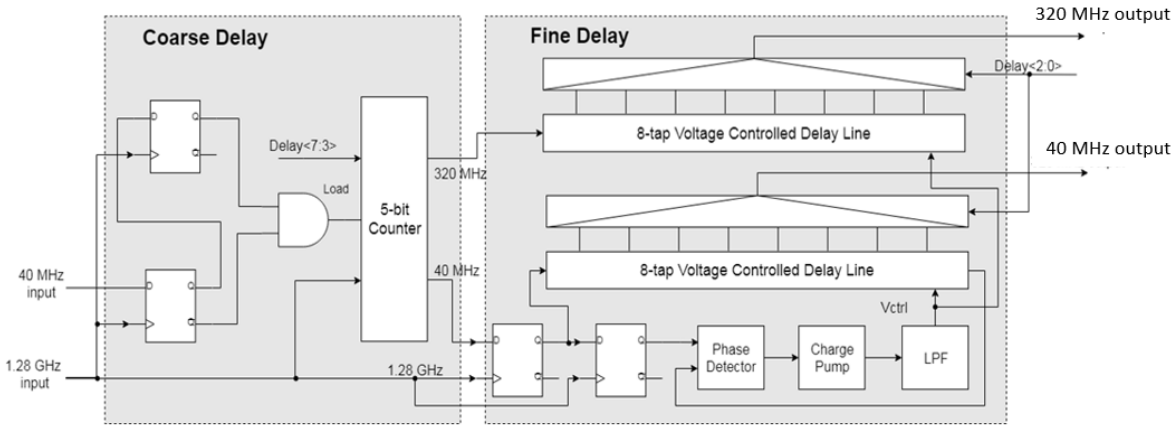

Figure 5.3.2-1 Block diagram of phase shifter

Table 5.3.2-1 IO interface definition of phase shifter

NO.	Name	Type	Description	Default

1	clk1G28	Analog input	1.28 GHz clock input of the phase shifter.	1.28G Hz
2	syncCK40	Analog input	40 MHz synchronized clock input of the phase shifter.	40M Hz
3	s<7:0>	Digital input	Phase selecting control bits, s<7:3> for coarse, s<2:0> for fine.	8'b0000000
4	dllEnableA	Digital input	Enable control for DLL, DFF and control voltage, active high.	1'b1
5	dllEnableB	Digital input	Enable control for DLL, DFF and control voltage, active high.	1'b1
6	dllEnableC	Digital input	Enable control for DLL, DFF and control voltage, active high.	1'b1
7	dllForceDown	Digital input	Force to pull down the output of the phase detector, active high.	1'b0
8	dllCapResetA	Digital input	Reset the control voltage of DLL to power supply, active high.	1'b0
9	dllCapResetB	Digital input	Reset the control voltage of DLL to power supply, active high.	1'b0
10	dllCapResetC	Digital input	Reset the control voltage of DLL to power supply, active high.	1'b0
11	dllCPCurrent<3:0>	Digital input	Charge pump current control bits, range from 0 to 15uA for charge and discharge.	4'b0001
12	clk40MOut	Digital output	Phase output of 40 MHz clock.	-
13	clk320MOut	Digital output	Phase output of 320 MHz clock.	-
14	dllLateA	Digital output	Lock status prompt.	-
15	dllLateB	Digital output	Lock status prompt.	-
16	dllLateC	Digital output	Lock status prompt.	-
17	VDD	Power	Power supply of the phase shifter, 1.2 V.	-
18	VSS	Ground	Ground of the phase shifter, 0 V.	-

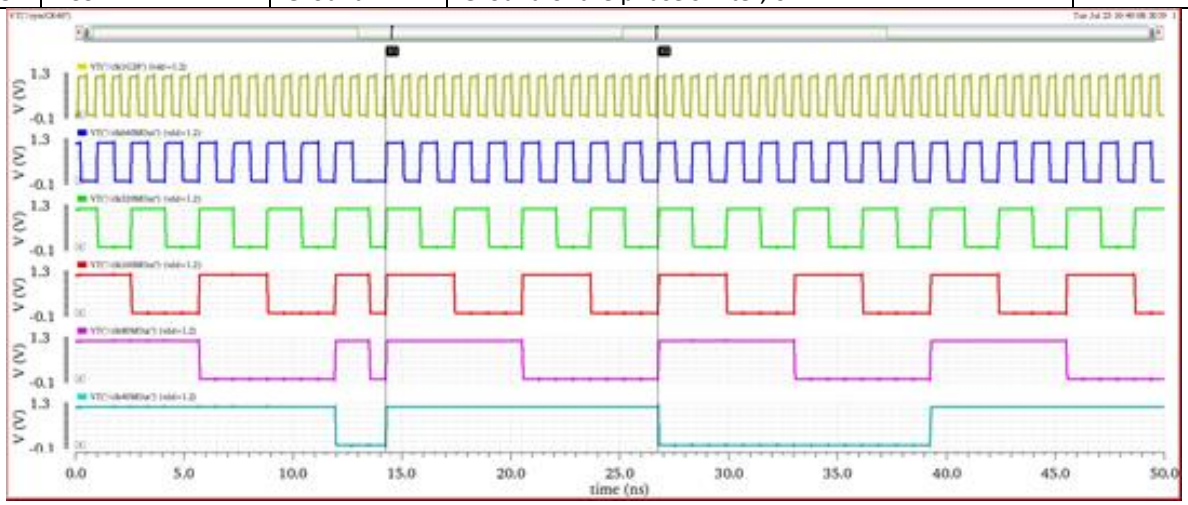

Figure 5.3.2-2 Post-layout simulation of coarse, Rising edge alignment

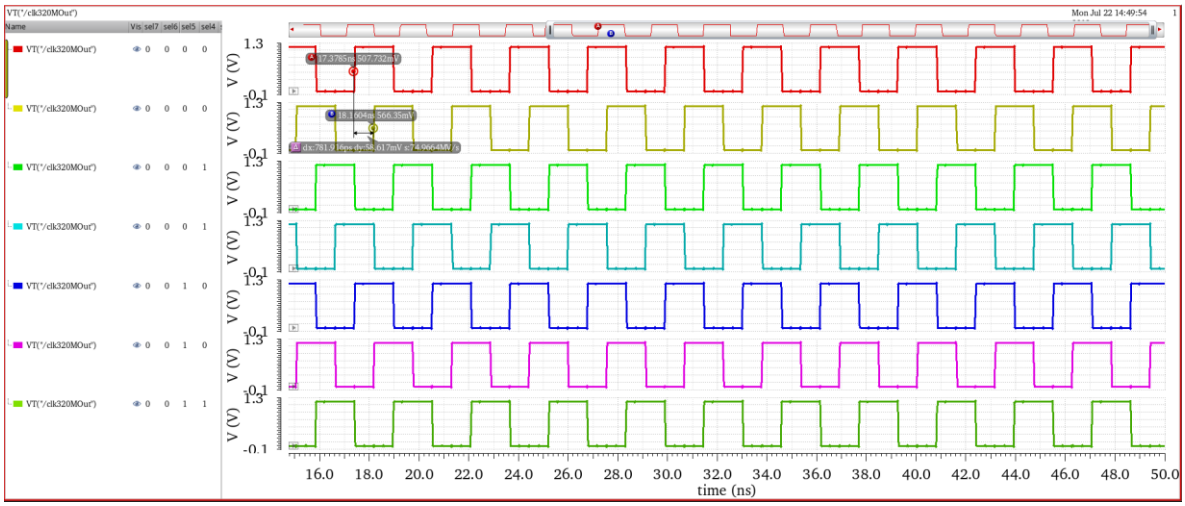

Figure 5.3.2-3 Simulation of coarse phase shifter ,781.25 ps phase shift by coarse

- **Reset of the phase shifter**

a. After power on, the control voltage should be reset LPF to VDD by setting the "dllCapResetA/B/C" to a high level. The reset time is less than 200 ns.
b. After resetting, the control voltage will continue to drop until the DLL is locked. Then it will change according to the switching of up and down signals in the charge pump.

5.3.3 TDC reference strobe generator

TDC reference strobe generator is a block designed for arbitrary-phase pulse generating. A 40 MHz clock is the reference clock. The rising edge of the 40 MHz clock is defined as the phase0. The synchronized 320 MHz clock and the delays of 40 MHz clock by DFF are used to generate the desired pulse. 8-bit control is adopted to select the output.

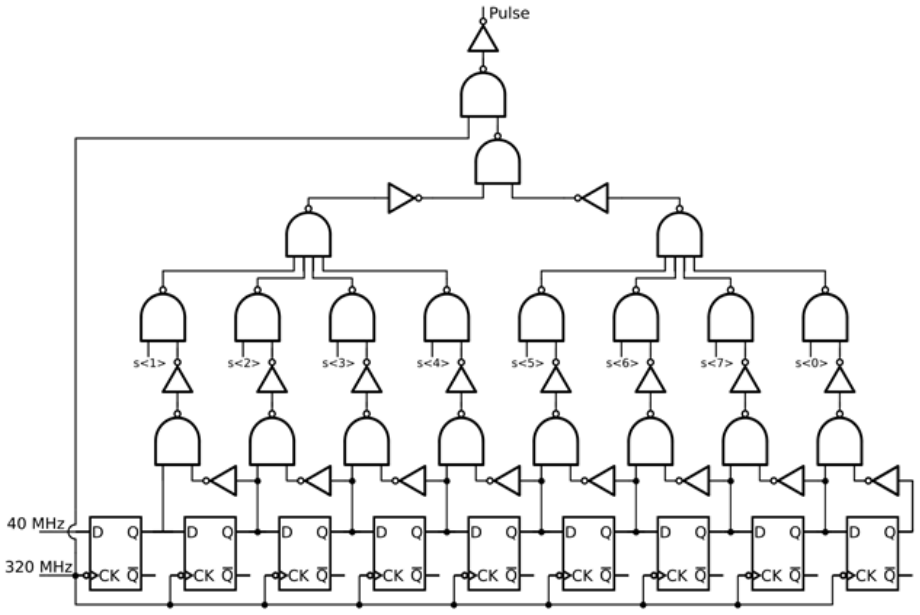

Figure 5.3.3-1 Block diagram of TDC pulse generator

Table 5.3.3-1 IO interface definition of TDC pulse generator

NO.	Pin Name	Type	Description	Default
1	CLK40M	Input	40 MHz reference clock.	
2	CLK320M	Input	320 MHz reference clock.	
3	s<7:0>	Input	320 MHz pulse phase select.	8'b00000011
4	clk40_delay	Output	Delayed synchronized 40 MHz clock.	
5	clk320_pulse	Output	Pulse output controlled by s<7:0>.	
6	VDD	Power	Power supply of TDC pulse generator, 1.2 V.	
7	VSS	Power	Ground of TDC pulse generator, 0 V.	

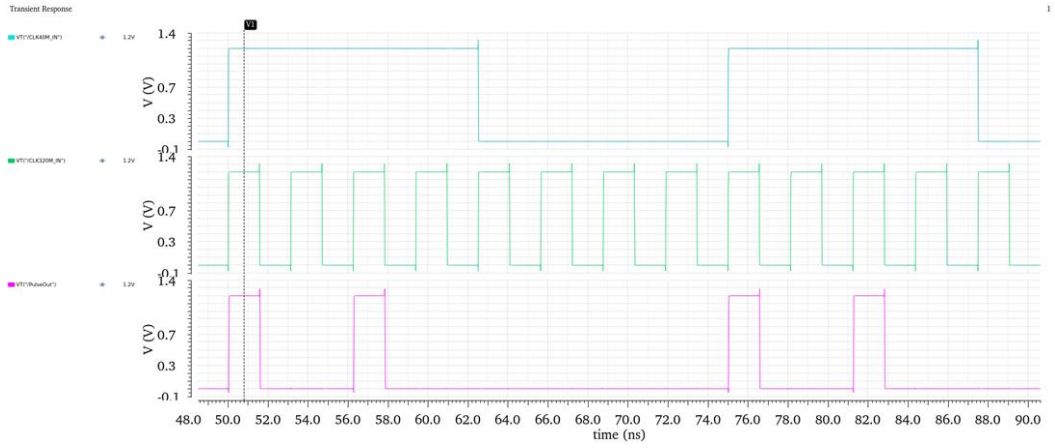

Figure 5.3.3-2 Post-layout simulation of TDC pulse generator, s<7:0> = 2'b00000101

5.4 DMRO

DMRO block takes 30-bit data as the input at the rate of 40 MHz, scrambles the input data with the polynomial of $X^{58}+X^{39}+1$, adds two bits as the header of the word(2'b10), and finally serializes 32-bit word to a 1.28 Gbps data stream. A PRBS7 generator is integrated for testability consideration. MSB goes first when delivering a word serially.

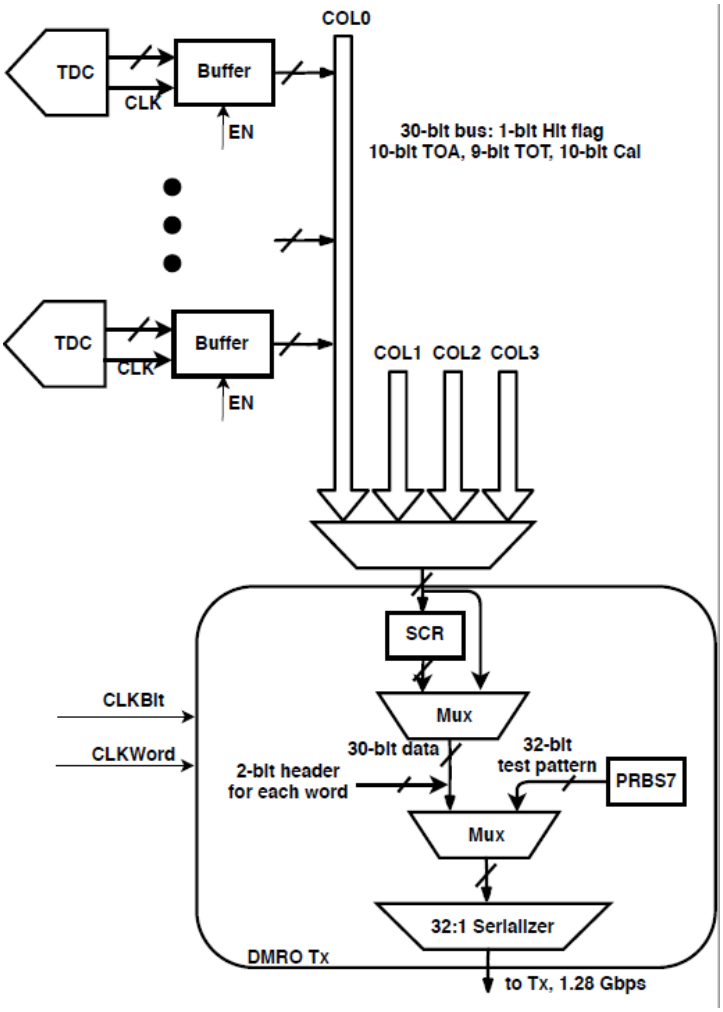

Figure 5.4.1 block diagram of the diagnostic mode readout scheme

Table 4.4 DMRO block pinout

Num.	Pin name	Type	Description
1	CLKBit	Digital input	1.28 GHz bit clock
2	CLKWord	Digital input	40 MHz word clock. Input data is latched at falling edges of this clock
3	RSTn	Digital input	Reset signal, active low. The logic is reset asynchronously at falling edge of RSTn and released synchronously at the first rising edge of CLKWord after RSTn becoming high.
4	REVData	Digital input	reversing input data, active-high.
5	REVCLK	Digital input	Reversing the clock used for input data latch, active-high. When REVData=0 data is latched at the rising edges of CLKWord, otherwise data is latched at the falling edges of CLKWord.

			Each time REVCLK changed, a reset pulse should be applied to RSTn.
6	ENScr	Digital input	Enable scrambling
7	TestMode	Digital input	Test mode input, active high. The PRBS7 is sent out in test mode (TestMode == 1) while the data is sent out in normal mode (TestMode == 0).
8	DataIn[29:0]	Digital input	30-bit data input
9	DataOut	Digital output	Serialized word.

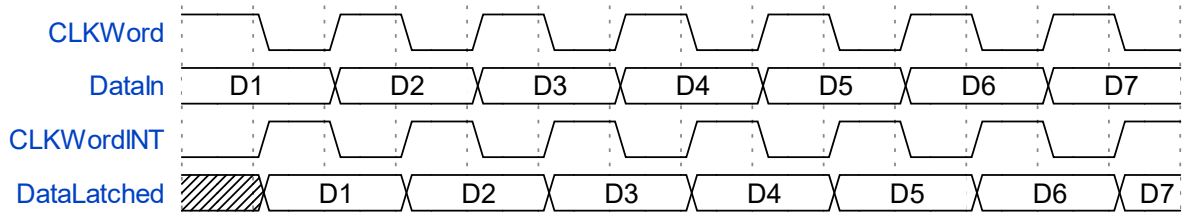

Figure 5.4.2 timing diagram of the DMRO input interface, REVCLK=1'b1

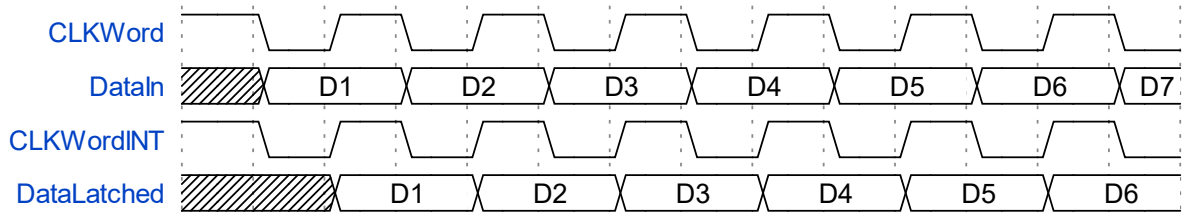

Figure 5.4.3 timing diagram of the DMRO input interface, REVCLK=1'b0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2'b10															Scrambled Data[29:0]																

Figure 5.4.4 data format of the DMRO data when the scrambler is on

5.5 Tx

Tx block takes the 1.28Gbps data whose amplitude is from 0 to vdd as input signal, translates the single-end signal into the signals in differential, finally drive 100 Ohm impedance. Its output amplitude is programmable by 3 bits control as well.

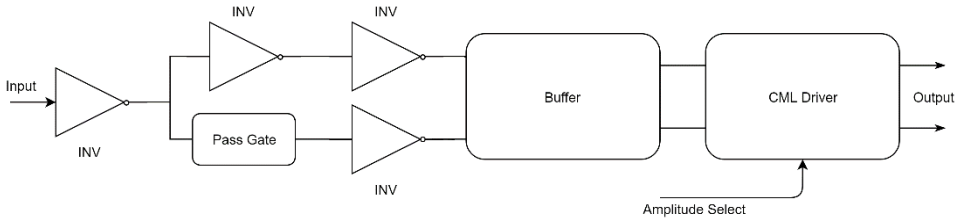

Figure 5.5.1 Diagram of Tx

Table 5.5.1 Tx block pinout

Name	Type	Description
IN	Input	0 – vdd input
Iin_CMLDriver	Input	Input 60uA current
AmplSel<0>	Input	3bits to select different output amplitude. 3b'000 = min amplitude(50m) 3b'111 = max amplitude(320m) Step size ≈ 40mV
AmplSel<1>		
AmplSel<2>		
disCMLDriver_BIASA	Input	When BIASA = 1 && BIASB=1 && BIASC=1, BIAS Circuit will be off.
disCMLDriver_BIASB		
disCMLDriver_BIASC		
on	Output	Output
op		
vdd	Input & Output	1.2V power supply
vss	Input & Output	Ground

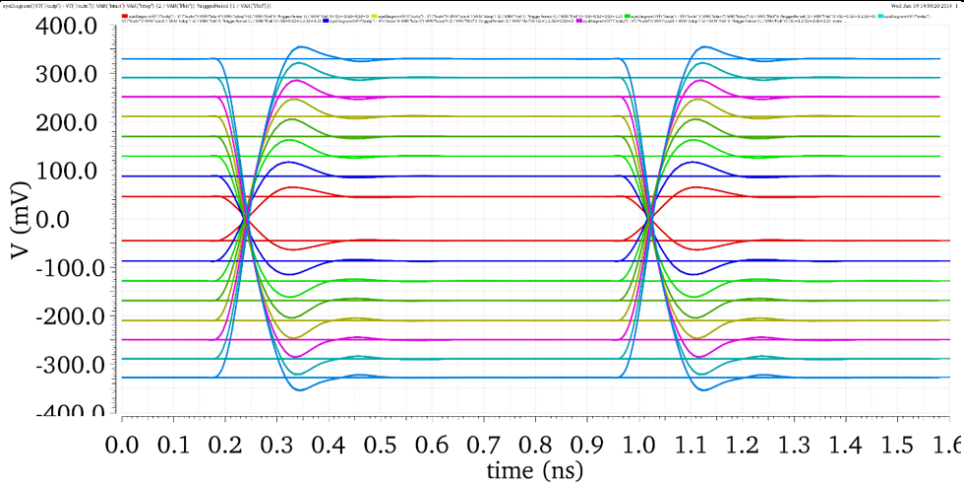

Figure 5.5.2 Post-layout Result of Tx

5.6 ERX

eRx is an IP block from lpGBT. It receives a differential signal and converts it into CMOS signal.

Parameter	Description	Min	Nom	Max	Units
V_{DD}	Supply voltage range	1.08	1.2	1.32	V
I_{DD}	Average current consumption		850		µA
V_{CMRX}	Common-mode voltage range[A]	70	600	1200	mV
V_{CM}	Common-mode set voltage[B]		$V_{DD}/2$		
$\|V_{ID}\|$	Differential voltage[C]	140	200	400	mV
V_{IDTH}	Differential input[C] high threshold			70	mV
V_{IDTL}	Differential input[C] low threshold	-70			mV
V_{IH}	Single-ended input high voltage		700	V_{DD}+200	mV
V_{IL}	Single-ended input low voltage	-40	500		mV
Z_{ID}	Differential input impedance	80	100	125	Ω
J_R	Random noise jitter			10[F]	ps rms
J_{PW}	Pattern or pulse width dependent jitter[D]			10[F]	ps
$T_{R/F}$	Output rise/fall time		30		ps
PSR	Power supply rejection			10[F]	ps/100mV
CMR	Common mode rejection			10[F]	ps/100mV
C_{CM}	Common mode termination capacitance		tbd.		pF
L_O	Output load		100		fF

[A] Common mode: $(V_{DP} + V_{DN}) / 2$
[B] For AC coupled signals
[C] Differential voltage: $V_{DP} - V_{DN}$
[D] Change of delay through the receiver with PRBS 2^{12}-1 @ 1.28Gbit/s or varying pulse width T_{PW} > 1ns
[E] For LVDS: 400mV
[F] If <=1ps possible (even with reduced input range), receiver could be used as hit receiver

Figure 5.6.1 Electrical specification of eRx

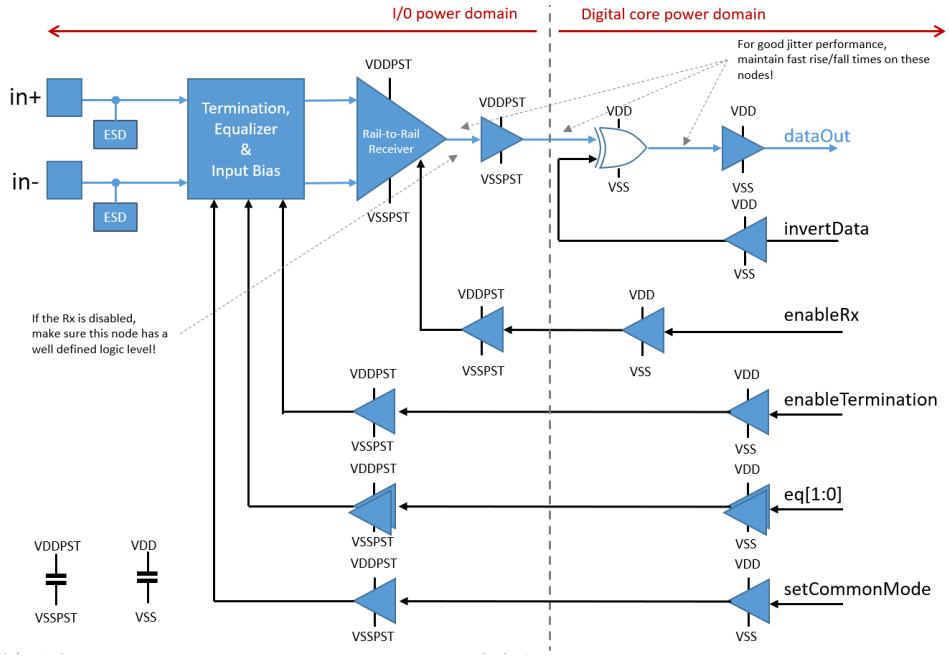

Figure 5.6.2 block diagram of eRx

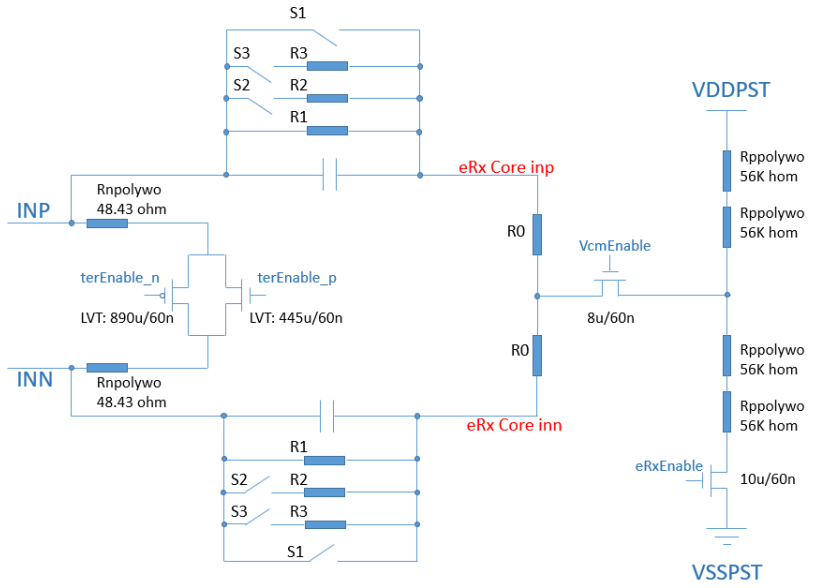

Figure 5.6.3 eRx input interface, C=730 fC, R1=3.45 kOhm, R2=5.3 kOhm, R3=1.8 kOhm

Table 5.6.1 eRx block pinout

Name	Type	Description
enableRx	Input	Enable eRx, active high
setCommonMode	Input	Set the input common mode voltage to vdd/2, active high
enableTermination	Input	Enable the 100 Ohm termination resistance, active high
in+, in-	Differential input	
invertData	input	Invert the signal, active high
Eq[1:0]	input	Internal equalization control
dataOut	Output	CMOS output

Table 5.6.1 eRx equalization control

Eq[1]	**Eq[0]**	**S1**	**S2**	**S3**	
0	**0**	1	x	x	0 Ω
0	**1**	0	0	1	R1//R3
1	**0**	0	1	0	R1//R2
1	**1**	0	0	0	R1

5.7 CHARGE INJECTION

The Charge injection block injects charge to the pre-amplifier for testability. It takes a step pulse control signal as input to generate the injected charge, and 5-bit input data to select injected charge, from 1 fC (5'b00000) to 32 fC (5'b11111). This block also can be tested with off-chip CSA to calibration injected charge.

The capacitor used to generate charge is 60 fC in ETROC1.

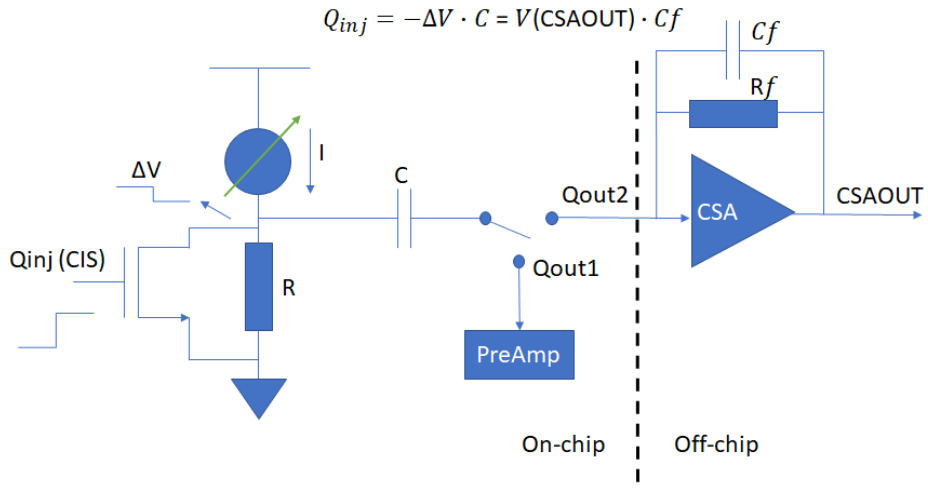

Figure 5.7.1 Block diagram of Charge Injection

Table 5.7 Charge Injection block pinout

Num.	Pin name	Type	Description
1	VREF	Analog input	Bias Voltage for Current Bias circuit
2	CIS	Digital input	Charge injection step pulse control signal
3	QSEL<4:0>	Digital input	Select injected charge, from 1 fC(5'b00000) to 32 fC (5'b11111) Typical charge is 6 fC (5'b00101)
4	EN	Digital input	Enable Charge Injection (onchip); Set low with minimum power consumption
5	QOUTSel	Digital input	Select charge output trace (default high: on-chip PreAmp) Output charge to off-chip CSA for testing when setting low.
6	TV1	Analog inout	Input voltage step pulse or output voltage for testing
7	Qout1	Analog output	Output signal to on-chip PreAmp
8	Qout2	Analog output	Output signal to off-chip CSA

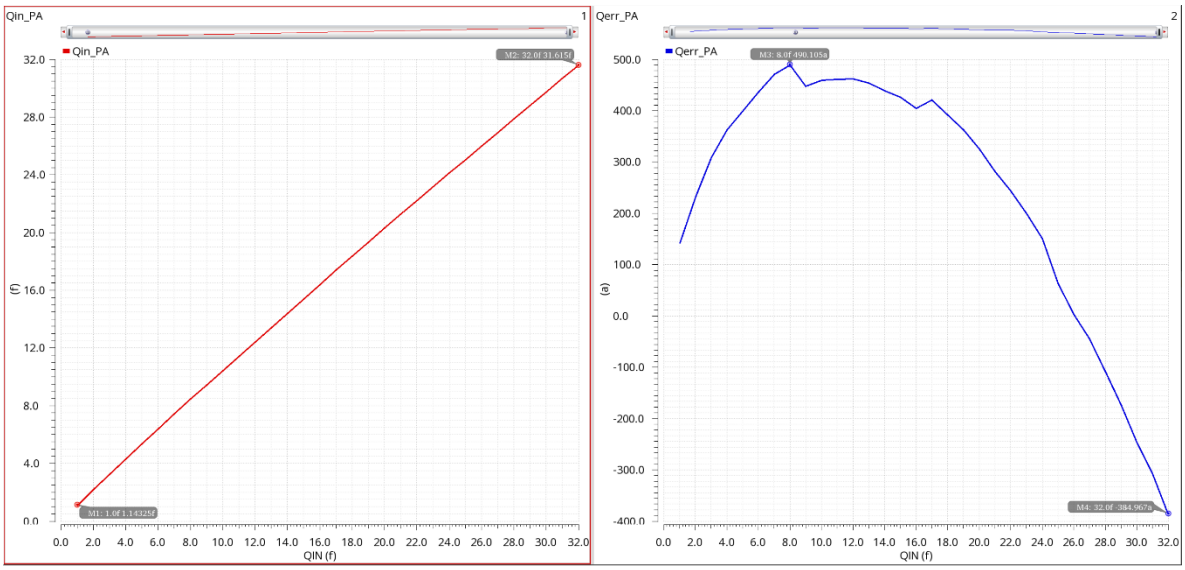

Figure 5.7.2 Simulated Injected charge vs input 5-bit control

5.8 READOUT TEST PATTERN GENERATOR

The purpose of readout test pattern generator (ROTestGen) is to generate test pattern for testing of SRO and DRO. ROTestGen outputs a configurable pattern so that the test pattern of each of 16 pixels could be different. The figure below shows a conceptual pixel block diagram including ROTestGen. A 4-bit input is used to config output pattern in ROTestGen. ROTestGen shares 4-bit LSBs with DAC which is bypassed in readout test mode (TestRO==1'b1).

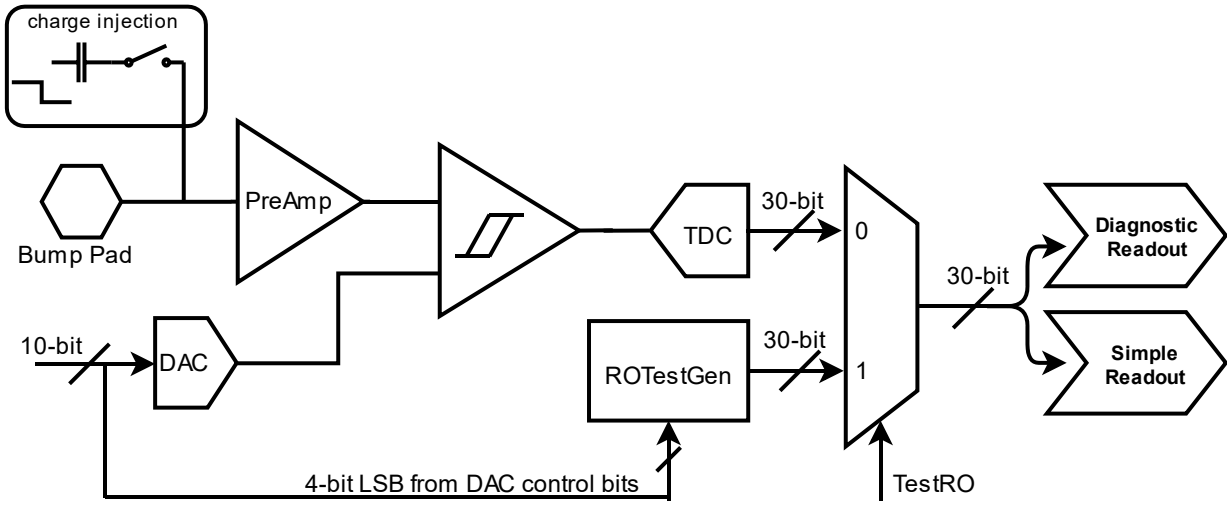

Figure 5.8.1 Block diagram of Readout test pattern generator

In the actual implementation, ROTestGen and the following mux are implemented in a single block, which is called ROTestCtrl. The 16-bit LSBs output (30-bit output in total) of ROTestCtrl is generated from a 16-bit counter. At rising edge of the input clock, the counter increases one. The 4 configuration bits are concatenated to the 16 counter bits, and 10 fixed bits locates at MSBs. The TestRO connects to enableMon in TDC. The pinout of ROTestCtrl is listed below.

Table 5.8.1 ROTestGen block pinout

Num.	Pin name	Type	Description
1	CLK	Digital input	40 MHz clock
2	CFGROTest<3:0>	Digital input	4 configuration bits used to distinguish pixel.
3	TestRO	Digital input	Control of readout test mode. When TestRO==1'b1, test pattern is sent for readout. When TestRO==1'b0, TDC output is sent for readout.
4	DataIn<29:0>	Digital input	30 bits TDC output data
5	DataOut<29:0>	Digital output	When TestRO==1'b1, test pattern is sent for readout. DataOut<15:0> is the 16-bit counter output. DataOut<19:16> == CFGROTest<3:0> DataOut<29:20> == 10'b1010101010 When TestRO==1'b0, TDC output is sent for readout.

6 DATA READOUT OF ETROC1

Two readout schemes are implemented in ETROC1. They are named diagnostic mode readout and simple readout, respectively.

6.1 DIAGNOSTIC MODE READOUT

In diagnostic mode readout, one of 16 pixels is selected and the test pattern or the date from the TDC is readout through DMRO block continuously at 30-bit per clock period. Since DMRO block adds 2-bit overhead per 30-bit word, the total data rate is 1.28 Gbps. The I2C registers, DMRO_COL[3:0] and OE_DMRO_Row[3:0], can be used to select the pixel to be readout.

6.2 SIMPLE READOUT

Simple readout is one of two readout schemes in ETROC1, through which the data stored in selected pixels(pixel) can be read out as a data frame with a predefined header and trailer. Each pixel includes a RAM which stores data from the TDC with width of 30-bit and depth of 256. Four pixels in a column share a bus, and four column-level buses connect to a module called SRO controller (simple readout controller). When normal running, WE=1, address increments, TDC values or test pattern (see test pattern generator section) are stored into the RAM buffers. When L1ACC occurs, WE is dropped (no data can be written into RAM), SRO controller sends the header word (SOF, start of frame) and then selects first enabled pixel. The address loops once reading out entire RAM buffer. Then it moves on to next enabled pixel, dumping out the RAM buffer. When the last word of the last enabled pixel is sent, the frame is ended up with the trailer word (EOF, end of frame). It returns to capture mode with WE=1. The simple readout shares the same DMRO block and the pads with diagnostic mode readout.

The I2C register, ROI (region of interest), specifies which pixels are enabled for readout. The readout order is Pixel 15, Pixel 11, Pixel 7, Pixel 3, Pixel 14, Pixel 10, Pixel 6, Pixel 2, Pixel 13, Pixel 9, Pixel 5, Pixel 1, Pixel 12, Pixel 8, Pixel 4, Pixel 0. E.g. ROI=16'h9A01 will cause pixels 15 (Row3Col3), Pixel 11(Row3Col2), 9 (Row2Col1), 12 (Row3Col0), and 0 (Row0Col0) readout in that order.

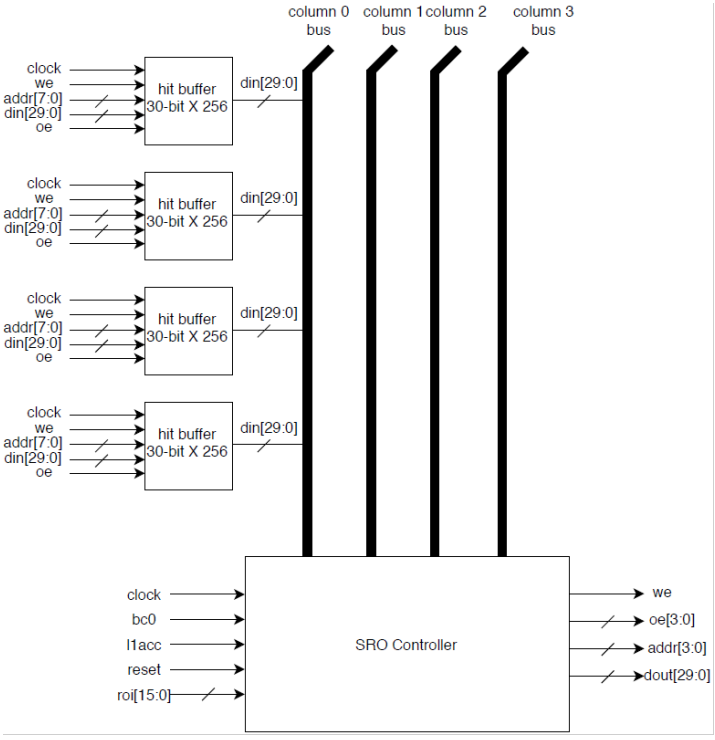

Figure 6.2.1 Block diagram of simple readout

18'h25555	12-bit L1ACC_ID	0-bit to 16 x 256 x 30-bit Frame Body. Length depends on ROI	30'h2EADBEEF
30-bit SOF			30-bit EOF

Figure 6.2.2 frame format of simple readout

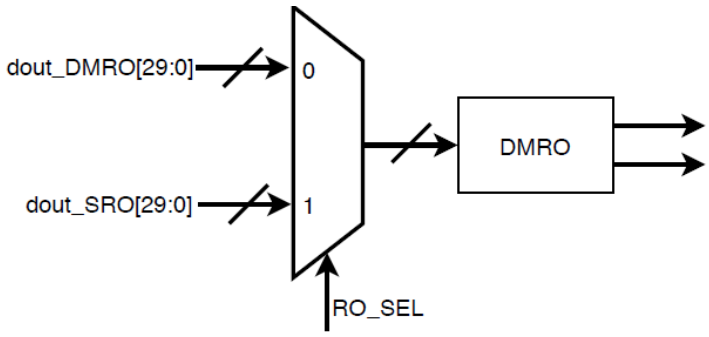

Figure 6.2.2 Block diagram of data path shared by two readout schemes

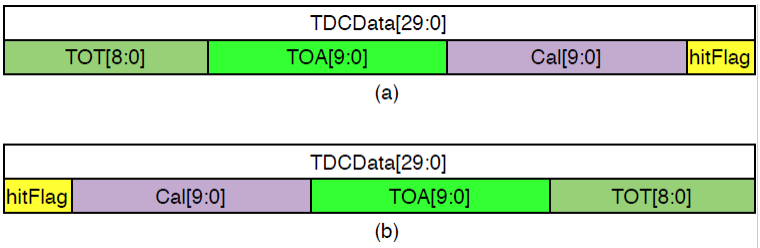

Figure 6.2.3 data format of 30-bit word from TDC: (a) data format of standalone pixel and pixel array, (b) data format of TDC test chip

P_0_0 index: 0	**P_0_1 index: 4**	**P_0_2 index: 8**	**P_0_3 index: 12**
P_1_0 index: 1	**P_1_1 index: 5**	**P_1_2 index: 8**	**P_1_3 index: 13**
P_2_0 index: 2	**P_2_1 index: 6**	**P_2_2 index: 10**	**P_2_3 index: 14**
P_3_0 index: 3	**P_3_1 index: 7**	**P_3_2 index: 11**	**P_3_3 index: 15**
Chip peripherals			

Figure 6.2.4 pixels map

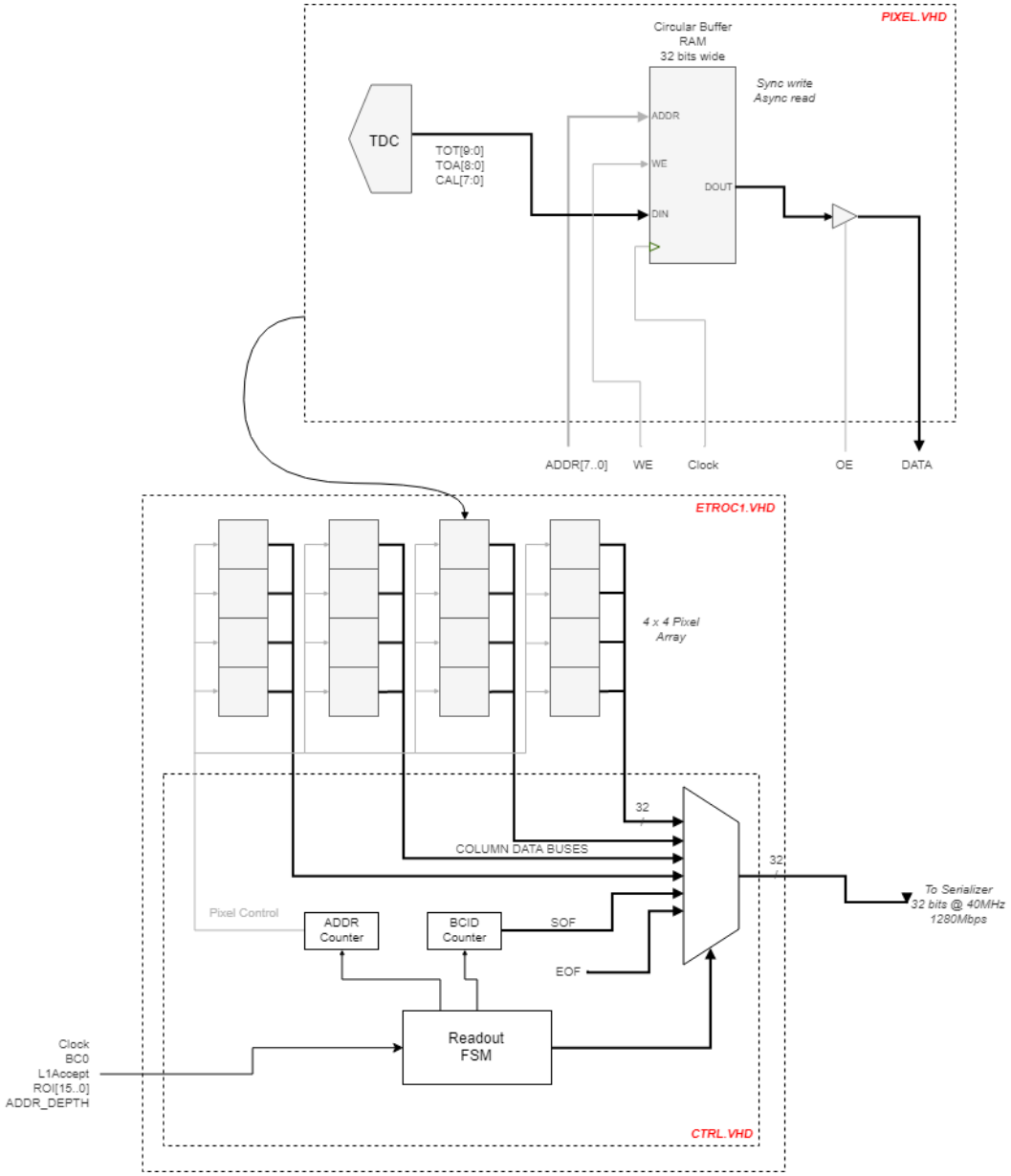

Figure 6.2.5 detailed block diagram of simple readout. 32-bit words have been changed to 30-bit to match with DMRO block. A 12-bit BCID counter increments as clock goes and can be reset when bc0 occurs. The instant BCID value will become part of SOF as L1ACC_ID when L1ACC occurs.

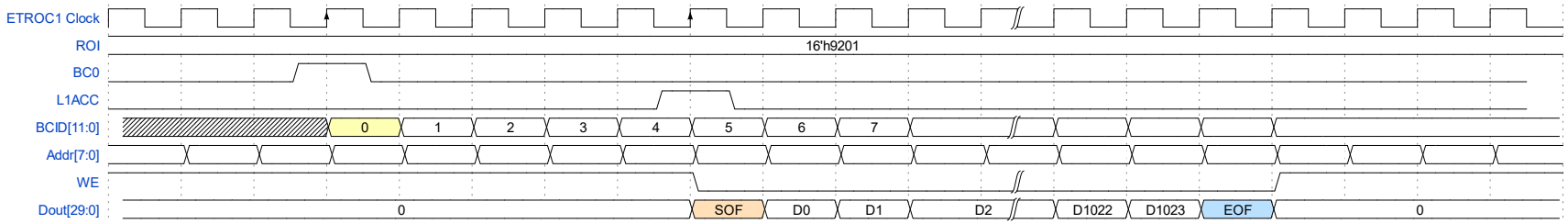

Figure 6.2.5 an example of simple readout sequence. In this case, the L1ACC_ID is 4 and the frame length is 1026 words including the SOF and EOF.