Module PCB Specifications

Andrew Peck, Daniel Spitzbart

June 10, 2022

1 Module Specifications

- Authors: Andrew Peck, Daniel Spitzbart
- Modification Date: 2022-06-10 21:28
- Status: This document is missing 26 pieces of information concerning 42 specifications
  - Specifications are **38.1% complete**.
- A pdf version of this document can be found here. Please check the timestamp to ensure it is up to date. The master copy of this document is an emacs org mode file found here.

Contents

2 Specifications

2.1 Description

The module PCB is a simple printed circuit board which will host two LGAD sensors, and two LGAD modules. To support these, it will have wire bond pads, a variety of passive components (capacitors and resistors), and a connector interface to attach to a Readout Board (RB).

- Documentation for the ETROC does not exist.

2.2 Layout

- We denote the "top" side of the PCB as that containing the sensor.
- We denote the "bottom" side of the PCB as that containing the module and BV connectors.

2.2.1 Sensor Placement

- The dimensions of a Sensor+ETROC assembly is UNKNOWN × UNKNOWN mm.
- The position of the two Sensor+ETROC assemblies are (positions relative to UNKNOWN):
  - x= UNKNOWN mm; y= UNKNOWN mm.
  - x= UNKNOWN mm; y= UNKNOWN mm.

2.2.2 Wire bonding

- A wire bonding diagram of an ETROC is shown in [1] and [2].
- The ETROC pinout is shown in [3].
- The pad pitch will be UNKNOWN mm.
- The pad aperture will be UNKNOWN × UNKNOWN mm.
- The pad aperture will be NSMD (non-solder-mask-defined) with the mask oversized by UNKNOWN mm.
- The wire bond pads will be located UNKNOWN mm from the edge of the ETROC (measured edge-to-edge).

[1] https://etl-rb.docs.cern.ch/files/2022-05-22-etroc-pinout/ETROC2bonding.pptx
[2] https://etl-rb.docs.cern.ch/files/2022-05-22-etroc-pinout/ETROC2bondingdiagramGerber.zip
[3] https://etl-rb.docs.cern.ch/files/2022-05-22-etroc-pinout/ETROC2-pinouts-table.xlsx

2.2.3 Grounding

- The RB will geometrically isolate analog and digital ground, with specified areas of the PCB filled by a digital ground pour, and others filled by an analog ground pour. The digital and analog grounds will be connected together at a single point. Alternatively, the grounds may be separated into ASIC domain vs. HV domain
  - A drawing of proposed grounding schemes are shown in [4].
  - Final grounding scheme is yet UNKNOWN
- The entire plane under the ETROC shall be grounded according to the aforementioned grounding scheme, with **no break** in the grounding for vias.
- The exposed ground surface shall be exposed gold (ENIG) with no solder mask for maximum flatness.

2.2.4 Fiducial Markings

- The module PCB will have on its top side 4 fiducial markers, composed of circles with crosses through them. These markers shall be placed with their centers 2.0 mm from the corners of the board. The markers should be clear of solder mask.

2.3 Connectivity

2.3.1 Readout Board Interface

1. Signal Interface The signal interface to the readout board will consist of:
   - The readout board will use connector part number UNKNOWN.
   - The pinout of the readout board connectors is UNKNOWN.
   - The placement of these connectors is UNKNOWN.
2. BV Interface The BV interface to the readout board will consist of 8 spring connectors (4 BV pads, and 4 BV return pads)
   - The BV to readout board interface will use connector part number TE 1551631-5, a spring connector with minimum working height of 0.6mm and maximum current of 0.5A.
     - Product page: `https://www.te.com/usa-en/product-1551631-5.html`
   - The spring connectors will be hosted on the RB, so the module need only to expose gold pads in the correct locations.
   - The placement of these connectors is UNKNOWN.

[4] `https://indico.cern.ch/event/1139028/contributions/4779384/attachments/2406930/4117689/ETROC2_Pinout_v2%20-%20Read-Only.pdf`

2.3.2 I2C

- The module carries I2C signals (SCL, SCK) from the readout board and distributes it to the 4 ETROCs in a star topology.
- The module PCB will provide independent I2C addresses for each ETROC on a module. Addresses will be 0/1/2/3 corresponding to the slot, and are set directly by wire bonds.
  - Addresses **will not** be set by resistors, and can not be modified.
  - The ETROC2 address pins have internal 40k pull-down resistors [5].
  - For ETROC2 waveform sampler, the I2C pins do not have integrated pull-ups/downs.
- The module PCB will **not** provide pull-up resistors on I2C lines. These will be provided by the host-system.
- A slot address will be set by the readout board, so I2C address bits '(2 3 4) will be connected from the module to the readout board.

2.3.3 Low Voltage

The module must receive +1.2V from the readout board, and distribute it to the ETROCs in a low inductance, low resistance path.

- Each module will receive two *possibly* independent +1.2V supplies.
  - They will not be connected together in any way on the module, but *may* be ganged together on the RB.

1. Decoupling
   - The module will provide decoupling capacitors on the +1.2V supplies. The power filtering network will be composed of:

     (a) UNKNOWN resistors of UNKNOWN values
   - Decoupling capacitors will be placed as close as possible to the ETROC, and follow standard practices to maintain low inductance connections.
   - Decoupling capacitors will be suitably rated to minimize DC bias effects.
   - To reduce temperature dependence, ceramics will be chosen where possible with minimal temperature dependence (e.g. X7R).

[5] https://etl-rb.docs.cern.ch/files/ETROC2-FAQs-June02-2022-short.pdf

2.3.4 Signal Connectivity

- Each module will receive two 320 MHz downlinks from the RB
- Each module will receive four 40 MHz clocks from the RB
  - The clocks shall be length matched and skewed such that for a multi-drop pair of lpGBTs, the clock and data are synchronized at each ETROC's input pads.
- Each module will have 2 uplinks operating at up to 640 Mbps.
- The module will host UNKNOWN temperature sensors, which will be monitored in the RB.

Signal	Direction	Description
1V2 0	IN	Power for ETROCS 1 and 2
1V2 1	IN	Power for ETROCs 3 and 4
DAQ Elinks [3:0]	OUT	
Trigger Elinks [3:0]	OUT	
Clock [3:0]	IN	
VREF [3:0]	OUT	
Temp [3:0]	OUT	
Addr [4:2]	IN	
Reset	IN	
WS Reset	IN	
BV [3:0]	IN	
BV Return [3:0]	OUT	
GND		

1. Bias Voltage

   The module will receive bias voltage from the readout board and distribute it to the modules.

   - BV will be a maximum of *negative* 550 volts [6].
   - The module will support 4 independent BV interfaces, to reduce to routing burden as well as to allow flexibility for module powering.

   (a) Decoupling
   - The BV may or may not be decoupled/filtered on the module PCB UNKNOWN

2.4 Mechanics

2.4.1 Outer Dimensions

- The outer dimension of the Module PCB will follow a rectangular shape, with dimensions of UNKNOWN $\times$ UNKNOWN.

[6] https://indico.cern.ch/event/1131302/contributions/4749462/attachments/2398248/4100919/heller_LGAD_survival_trento_march2022.pdf

2.4.2 Screw Holes & Sizes

- The Module PCB will have 2 mounting holes of diameter 2.2 mm, centered along the vertical axis of the board, offset from the edge by 1.650 mm.

2.4.3 Standoff / mounting mechanics

- The module PCB will have a surface mount standoff to allow affixing it securely to the readout board. It will be place in UNKNOWN.

2.4.4 Thickness

- The Module PCB will be 0.5mm thick with a manufacturing specification of $\pm$ 10%.

2.4.5 Drawings

- A drawing of the Module PCB is available at UNKNOWN.
- A drawing of the ETROC and sensor is available at **??**.

2.4.6 Mechanical Interface

- the module shall be aligned to the Readout Board using an UNKNOWN keying mechanism

2.5 History

Date	Author	Change
2022/03/14	AP	Initial
2022/05/19	AP	Specify bias voltage and downlink data rate
2022/05/31	AP	Add final-not-final ETROC pinout/bonding
2022/05/31	AP	Add ETROC grounding / mechanical diagram
2022/06/09	AP	Updates to module signal assignments